



B85H3-M3

Rev : 1.0

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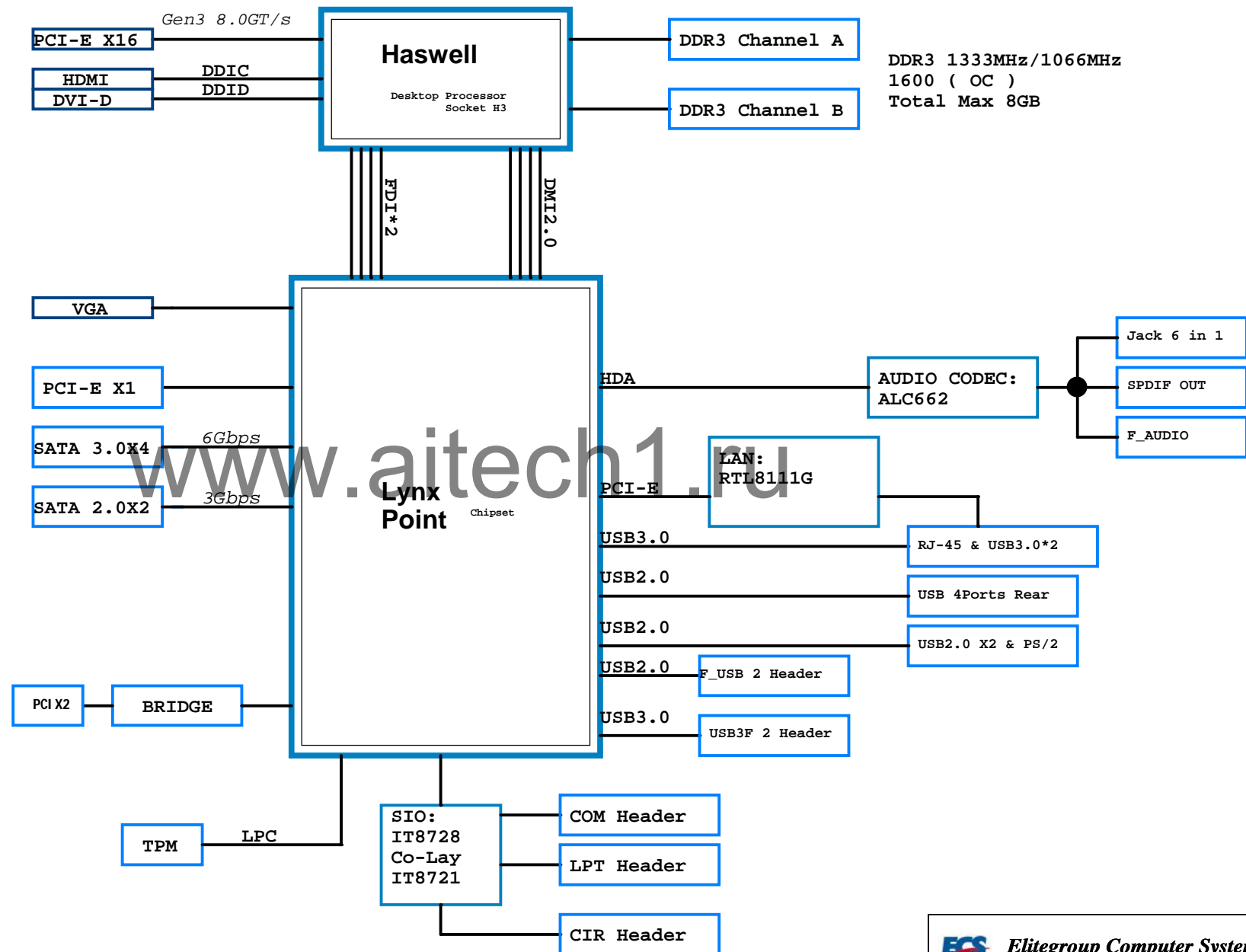
REVISION HISTORY:

Rev	Date	Notes
VA	2011 0820	Initial version
VA	2011 1015	For memroy, Change DDR3*4 to DDR3*2
VA	2011 1016	Change Audio IC from ALC892 to ALC662
VA	2011 1017	ME Disable change to 2pin
VA	2011 1017	DEL PCI-EX4 and ADD PCI2
VA	2011 1018	Change SATA3.0 X2 to SATA2.0 X2
VA	2011 1019	Modify USB Ports.
VA	2011 1023	HDMI&DP co-lay => HDMI Only.
VA	2011 1023	Add 3 pin PWR_FAN,remove smart fan function;Add 3 PIN SYS_FAN
VA	2011 1031	Add GPIO to adjust V_DIMM voltage

- NOTE:**
1. Model Code:
 2. Modified from H87H3-M V:A

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PCH-GPIO function

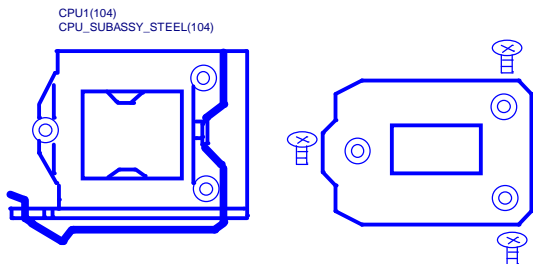
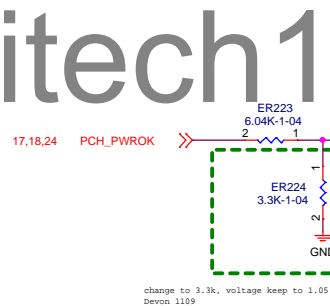
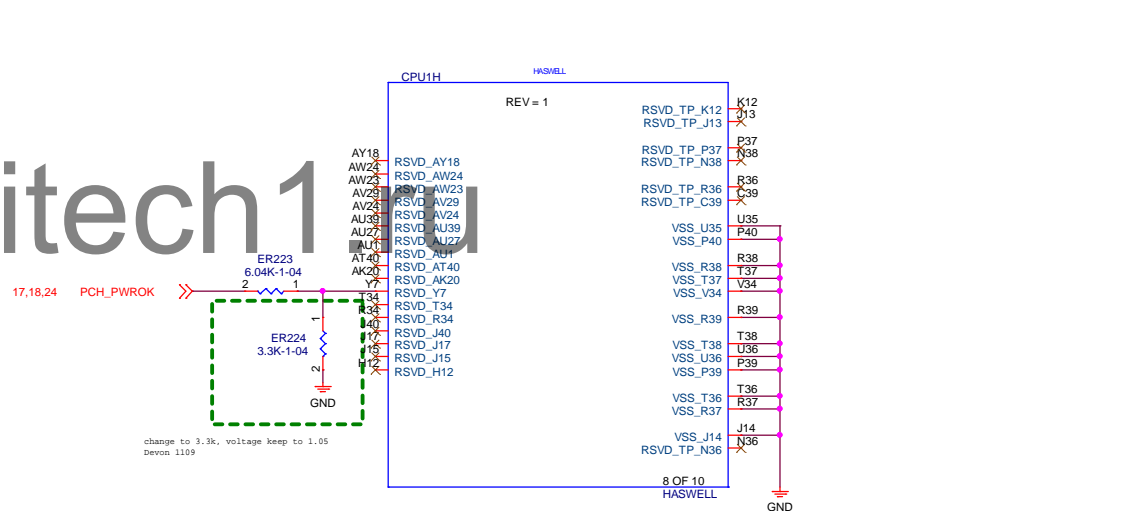
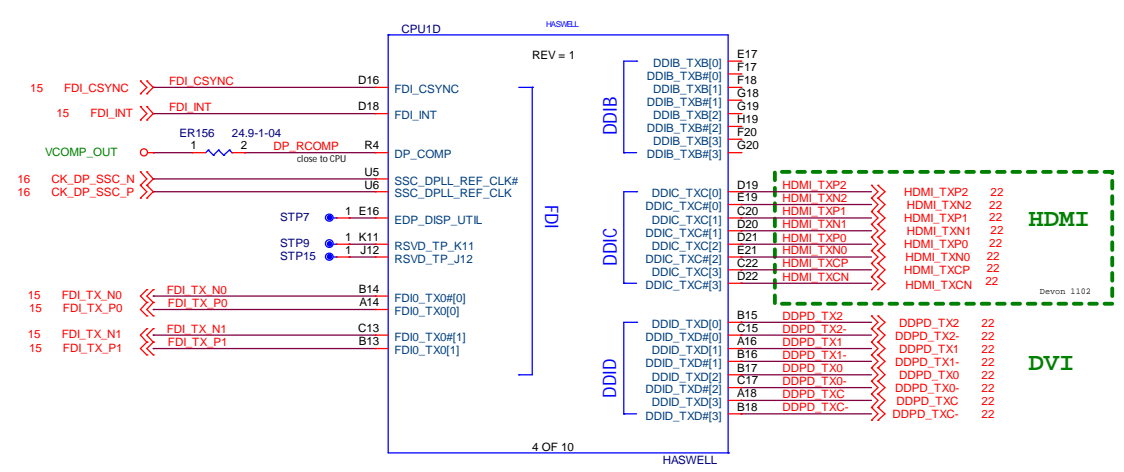
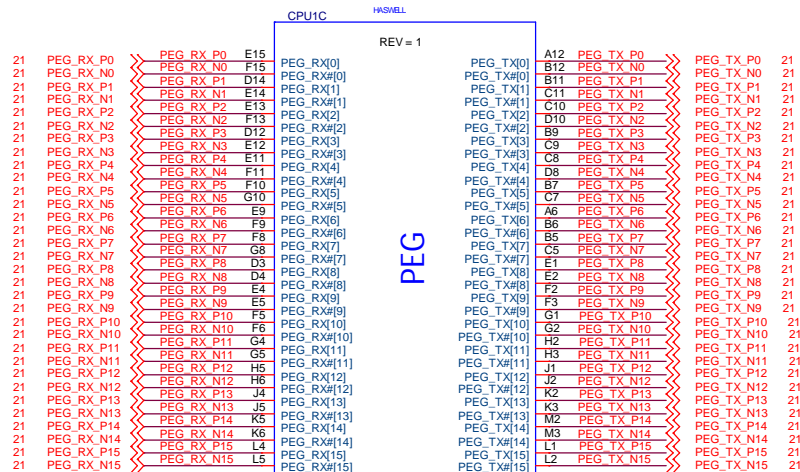
Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	case open(reserve)	GPI
GPIO13	3VSB	LPC_PME	GPI
GPIO24	3VSB	USB_5VDUAL control	GPO
GPIO72	3VSB	USB_5VDUAL control (reserve)	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	LAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO68	VCC3	TP_VGA	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	GPIO
GP33	ATX_3VSB	SUSACK#	GPIO
GP34	ATX_3VSB	SUSWARN#	GPIO
GP55	ATX_3VSB	DPWROK	RSMRST#
GP41	3VSB	RSMRST#	PWROK2
GP63	3VSB	3VSB SW_MINI	GPIO
GP35	3VSB	LED0	GPIO
GP37	3VSB	LED1	GPIO
GP72	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP75	VCC3	BOM detect	GPIO
GP76	VCC3	BOM detect	GPIO

Interrupt mapping

Function	INT# port	PCle*1 port	Device
LAN	INTC#	port 3	Clarkville or RTL8111DP
PCIEX1	INTD#	port 4	LPT integrate
PCIEX4	INTA#/B#	port 5-8	LPT integrate
mini-PCIE	INTB#	port 2	LPT integrate
SATA	INTB#	NA	LPT integrate



CPU steel (T/U phase)
PN:20-800-005711 CPU SOCKET STEEL SUBASSY.STEEL...LGA 1155/1156P.W/BACK PLATE,CAP.LOTES

CPU socket (SMD phase)
PN:11-018-115128 SOCKET.CPU..LGA 1150P SMD..15u...BLACK.ACA-ZIF-138-P01...HF.LEAD-FREE.LOTES

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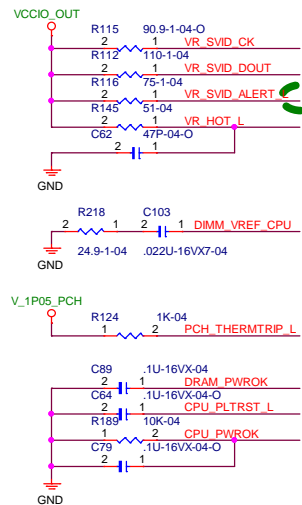
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Date: **Tuesday, May 28, 2013**

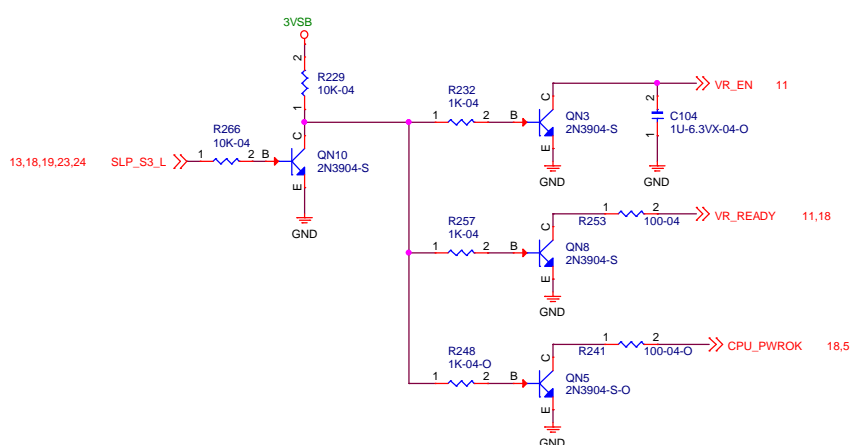
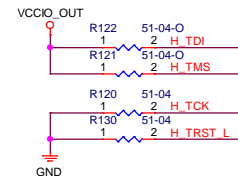
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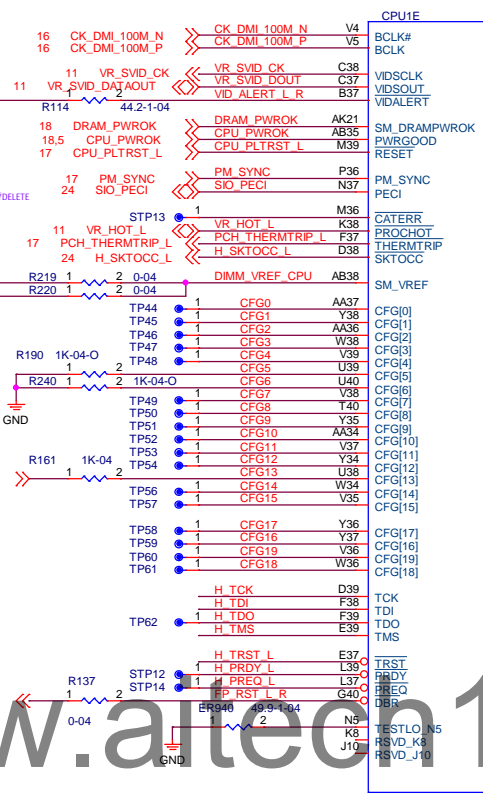
Change VID_ALERT_L_R to VR_SVID_ALERT_L
Devon 1119

CPU_THERMTRIP_L change PCH_THERMTRIP_L

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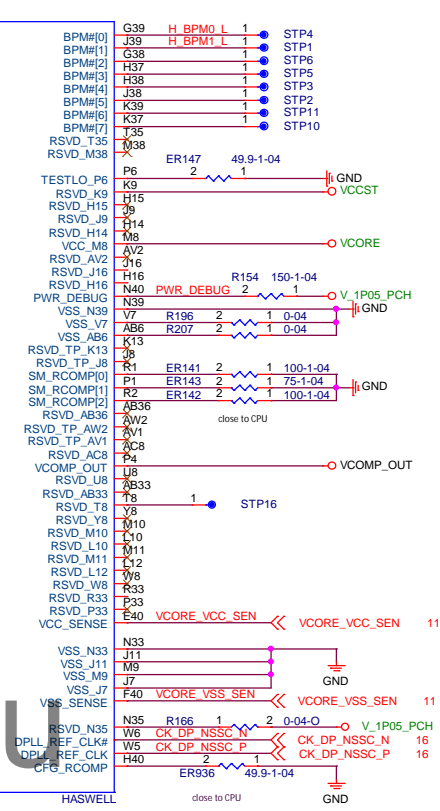


Power Down Sequencing Circuit



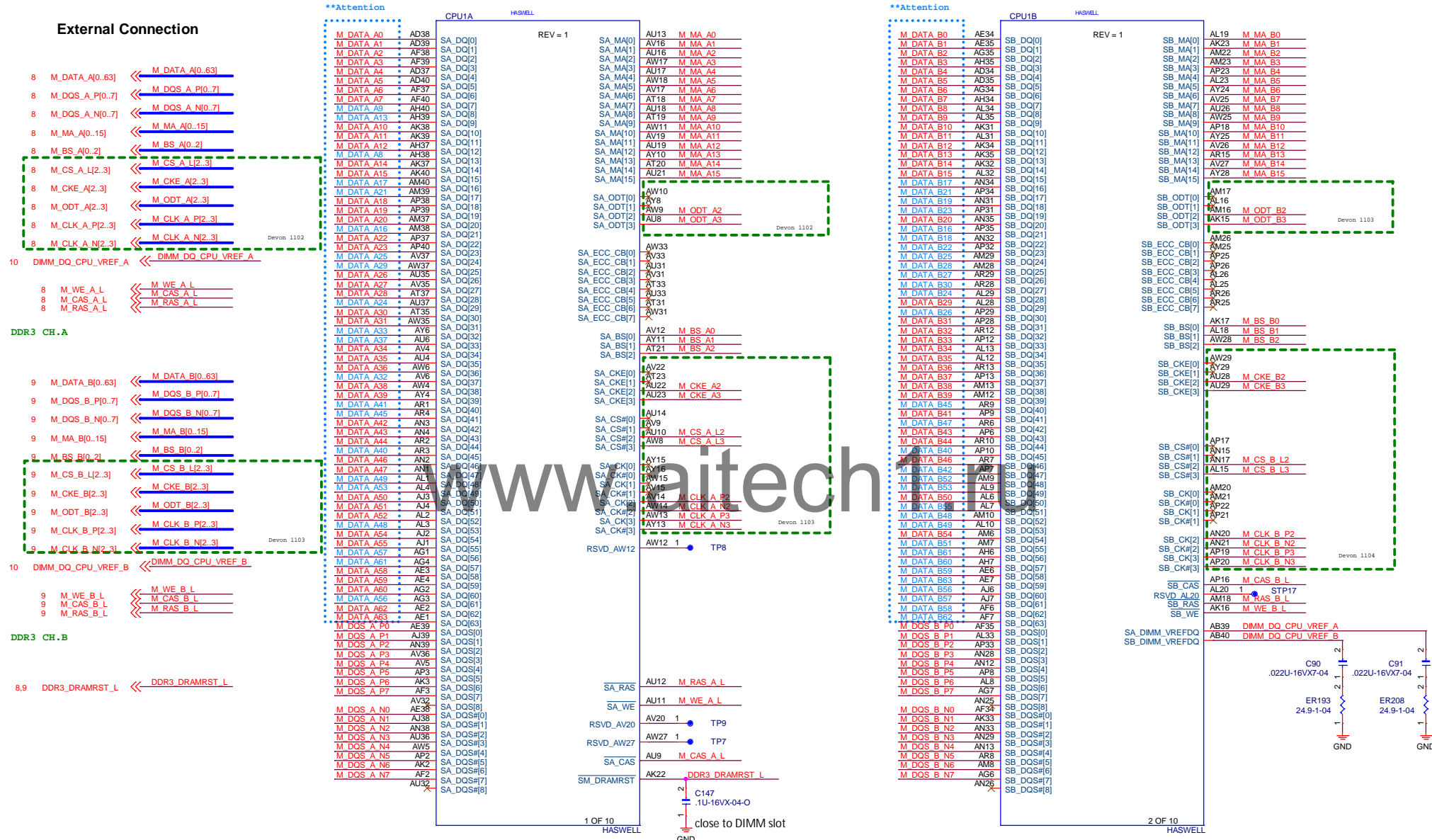
CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	CFG6	CFG5
1x16	1	1
2x8	1	0
Reserved	0	1
X8,X4,X4	0	0



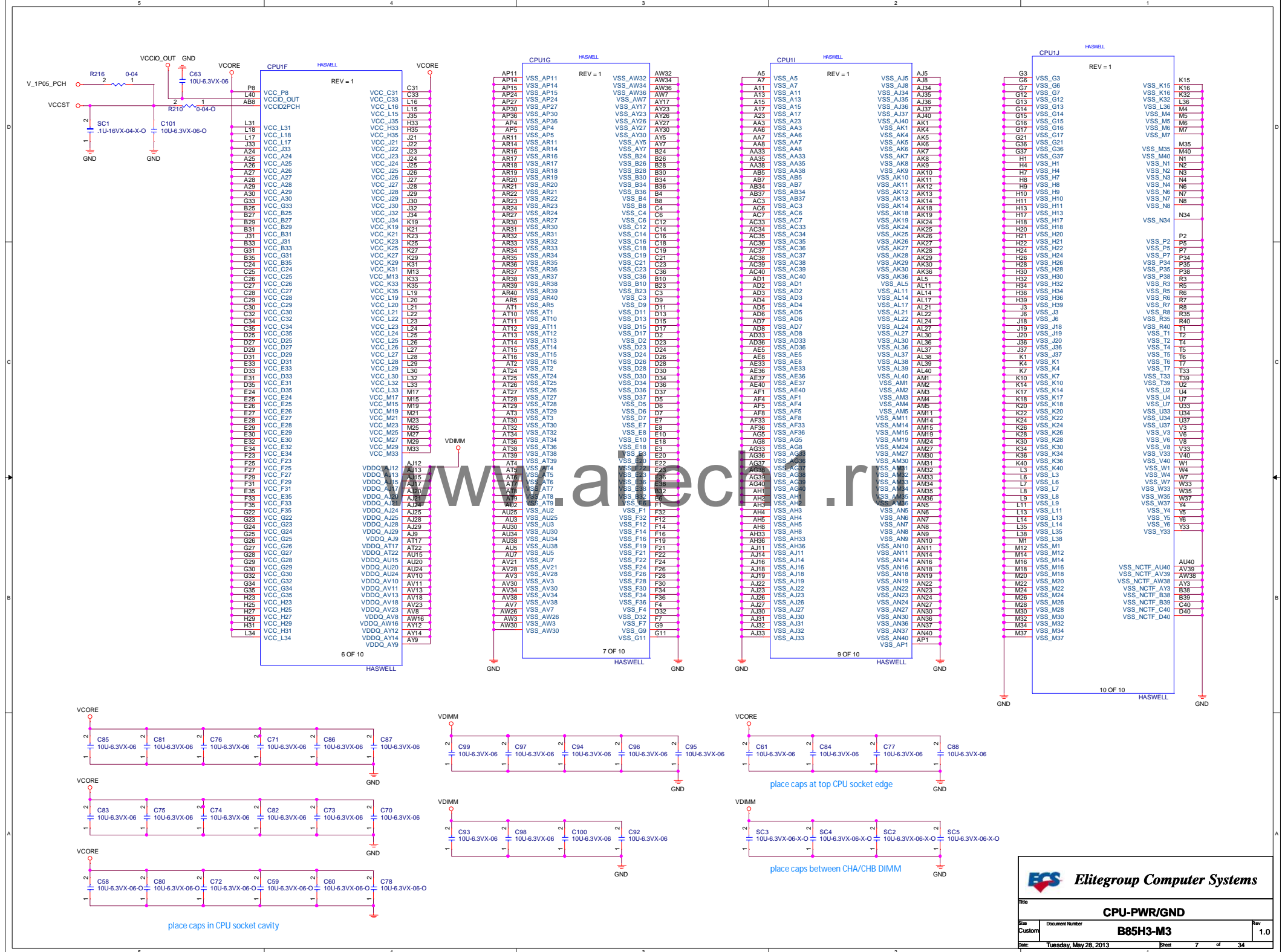
CFG[1:0]: Reserved configuration lane.
 CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
 1 = Normal operation
 0 = Lane numbers reversed.
 CFG[3]: MSR Privacy Bit Feature
 1 = Debug capability is determined by
 IA32_Debug_Interface_MSR (0xC80) bit[0]
 0 = IA32_Debug_Interface_MSR (0xC80) bit[0]
 default setting overridden
 CFG[4]: Reserved configuration lane.
 CFG[6:5]: PCI Express* Bifurcation:
 CFG[19:7]: Reserved configuration lanes.

External Connection



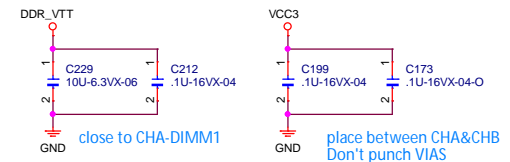
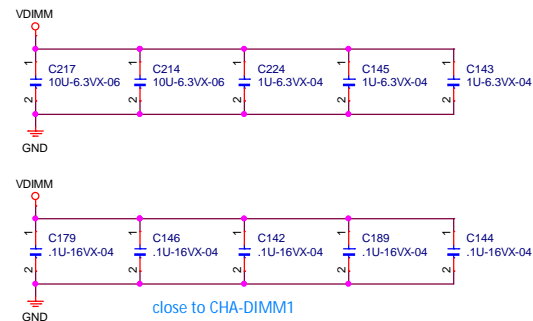
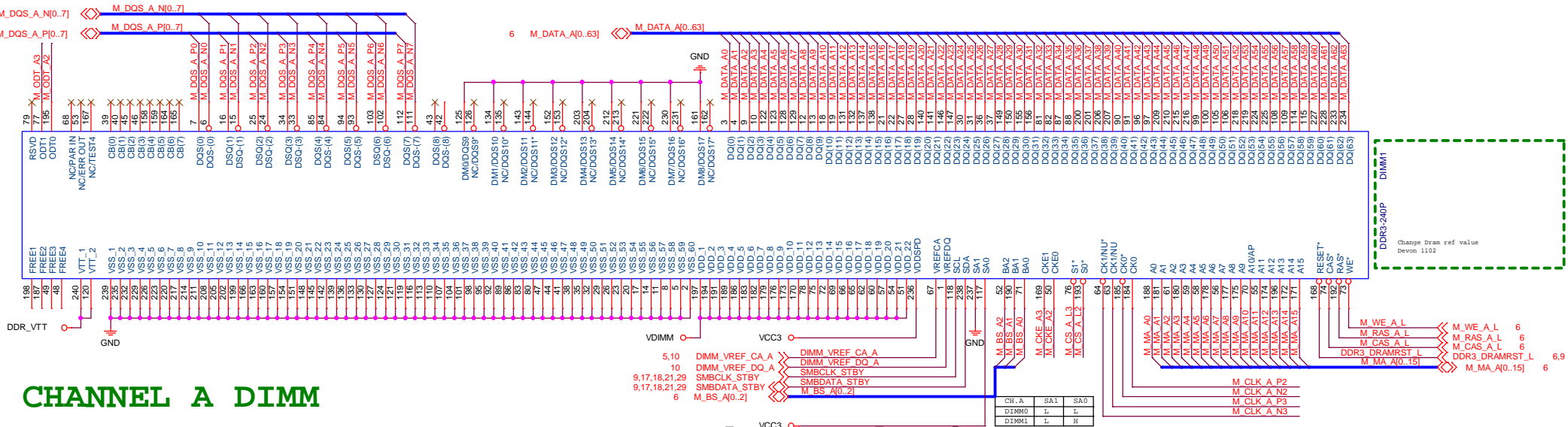
NC M_ODT_A[0..1], M_CKE_A[0..1], M_CS_A_L[0..1], M_CLK_A_P[0..1], M_CLK_A_N[0..1]
Devon 20121016

NC M_ODT_B[0..1], M_CKE_B[0..1], M_CS_B_L[0..1], M_CLK_B_P[0..1], M_CLK_B_N[0..1]
Devon 20121016



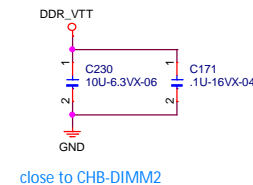
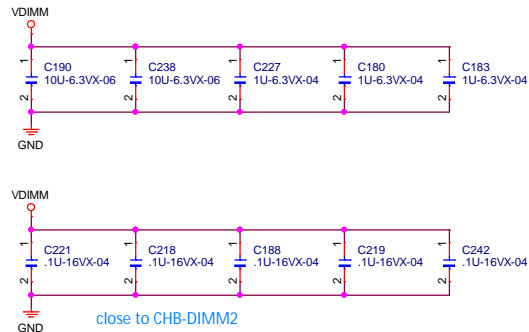
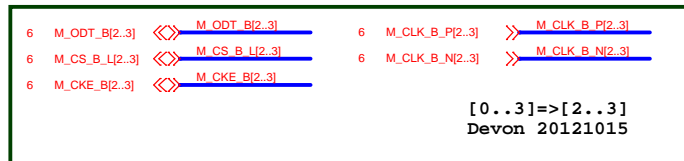
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CHANNEL A DIMM



CHANNEL B DIMM

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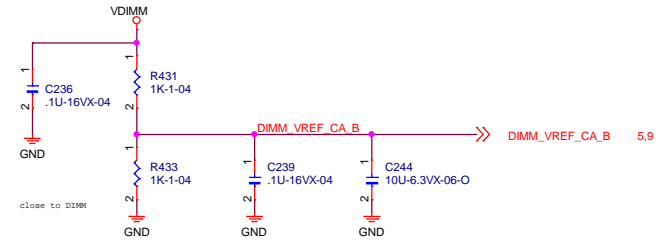
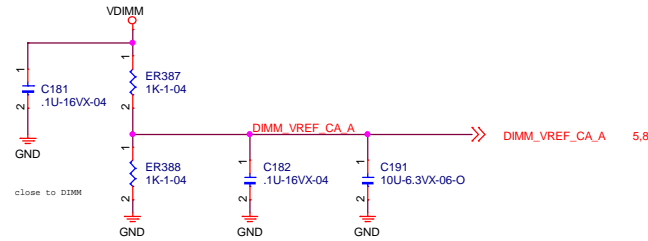
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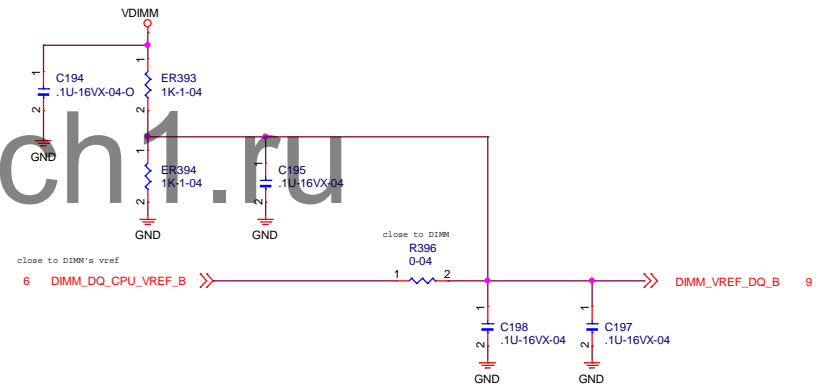
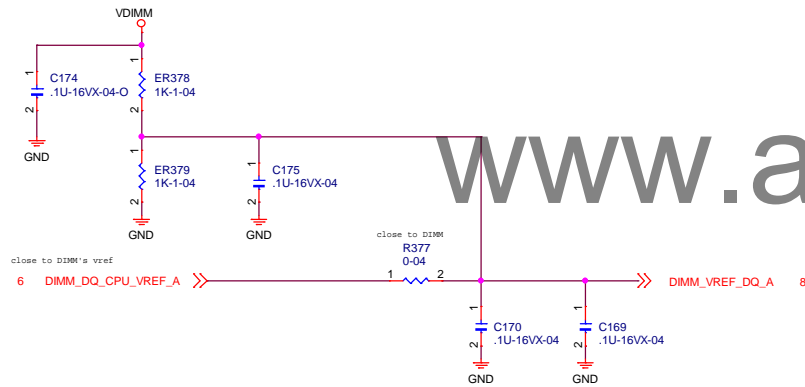
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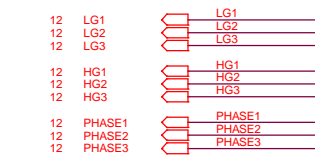
DIMM_VREF_CA Circuit



DIMM_VREF_DQ Circuit

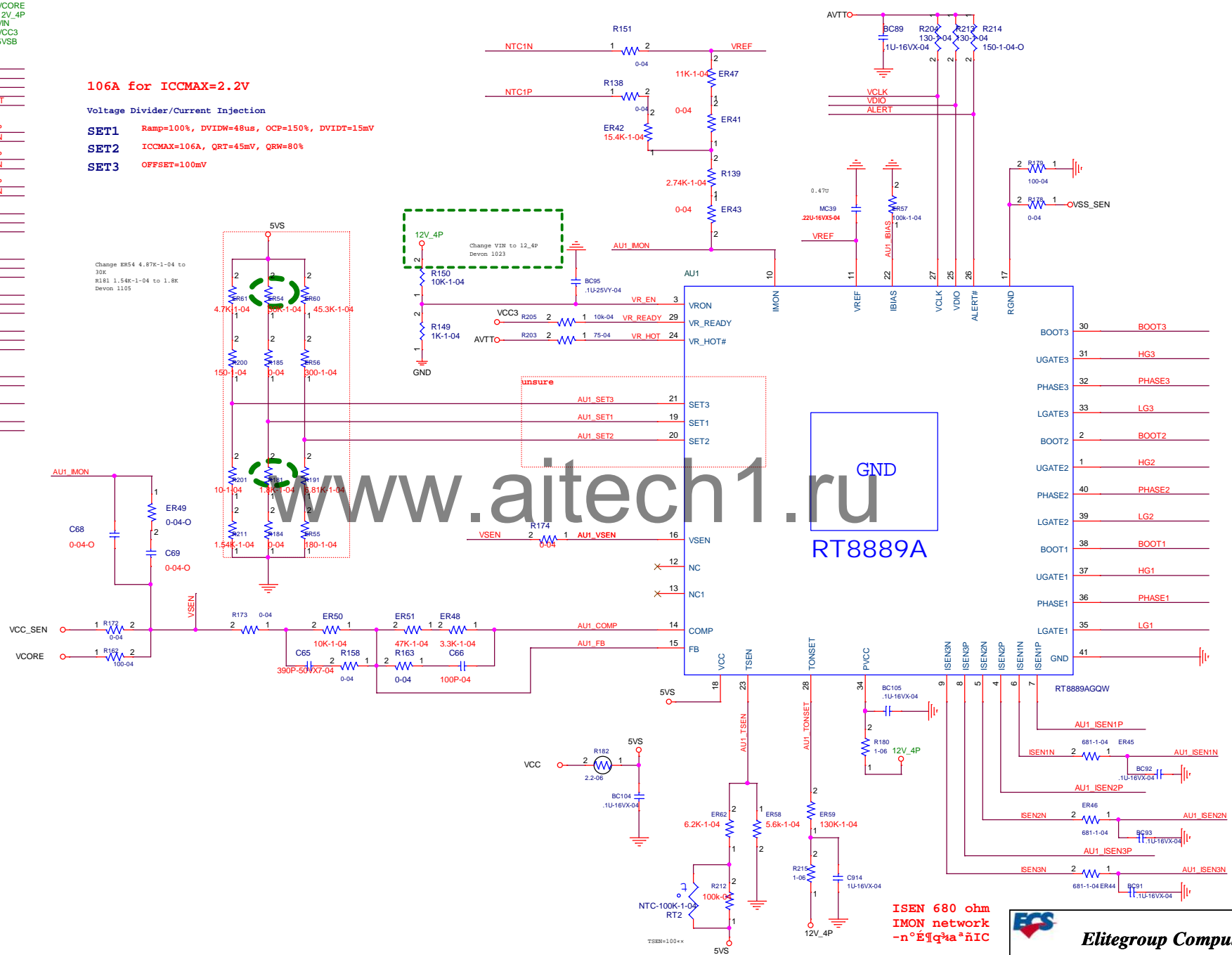


External Connection



Voltage Divider/Current Injection

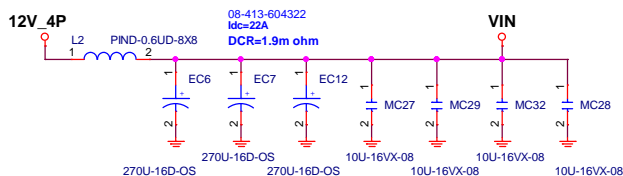
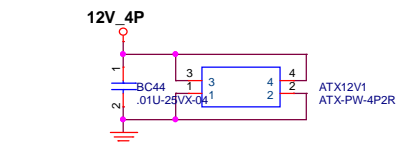
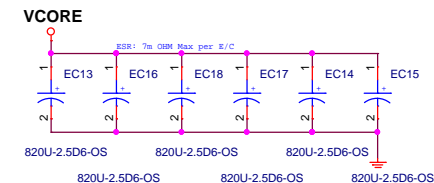
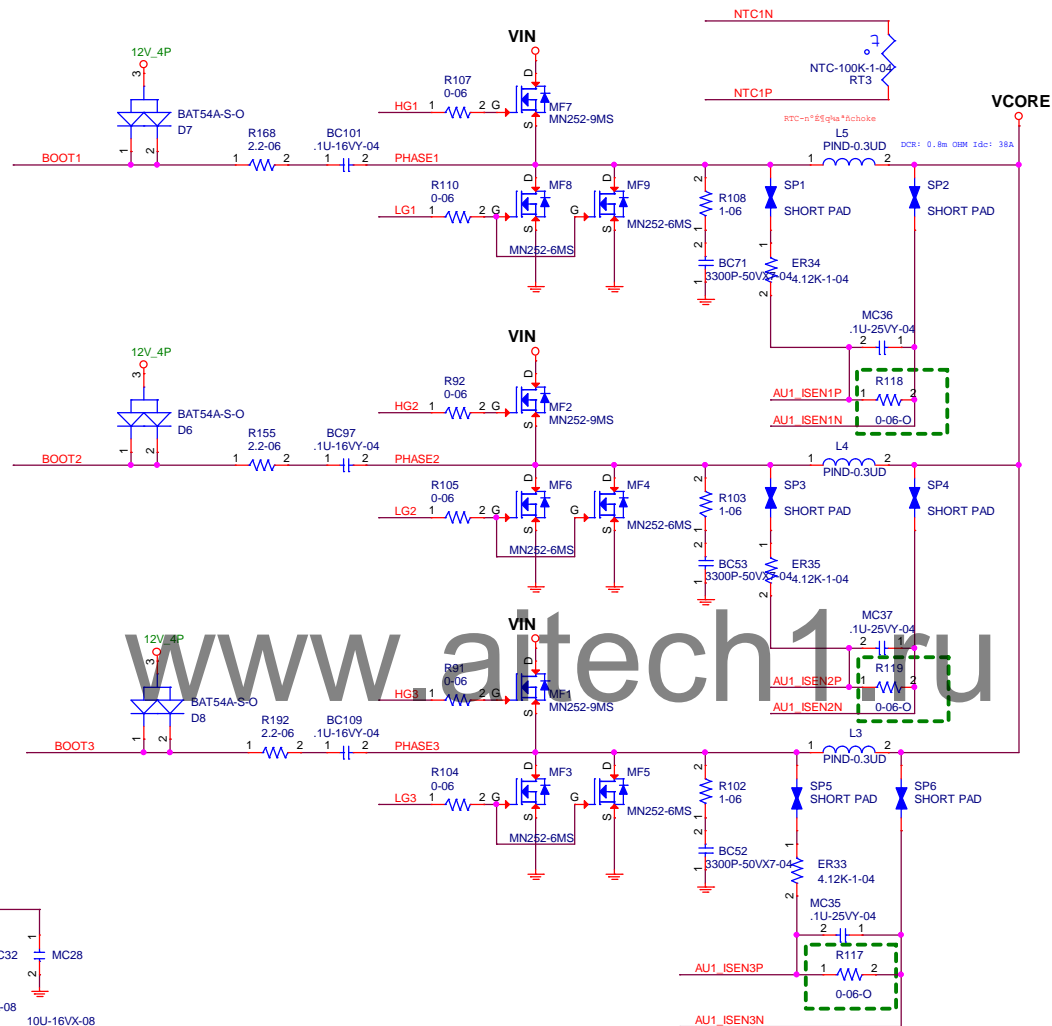
SET2 ICCMAX=106A, QRT=45mV, QRW=80%



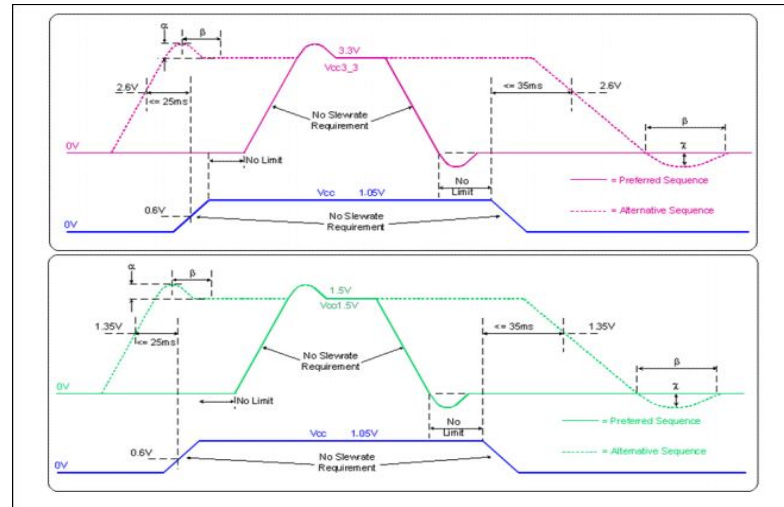
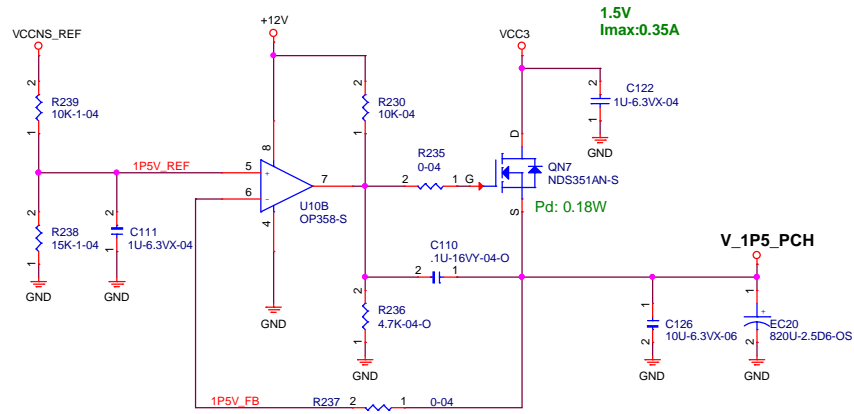
External Connection

VCORE ○ ○ VCORE
12V_4P ○ ○ 12V_4P
VIN ○ ○ VIN

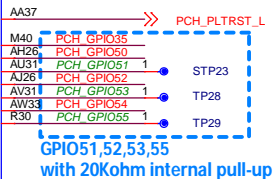
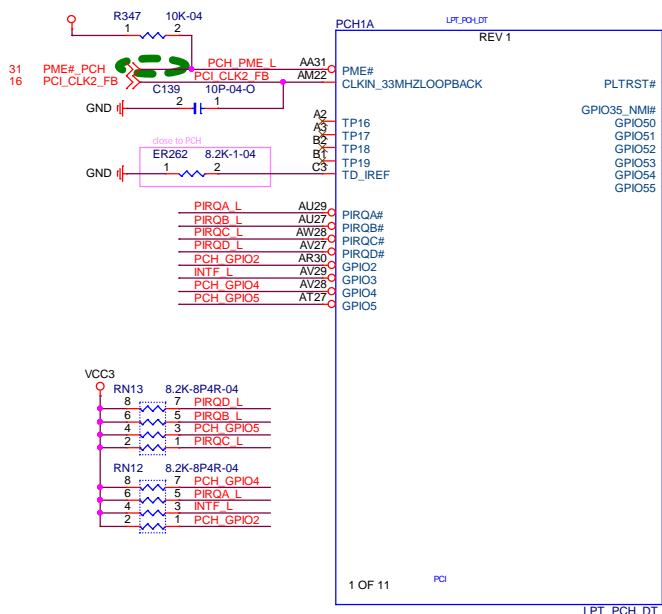
11	AU1_ISEN1P	AU1_ISEN1P
11	AU1_ISEN1N	AU1_ISEN1N
11	AU1_ISEN2P	AU1_ISEN2P
11	AU1_ISEN2N	AU1_ISEN2N
11	AU1_ISEN3P	AU1_ISEN3P
11	AU1_ISEN3N	AU1_ISEN3N
11	BOOT1	BOOT1
11	BOOT2	BOOT2
11	BOOT3	BOOT3
11	LG1	LG1
11	LG2	LG2
11	LG3	LG3
11	HG1	HG1
11	HG2	HG2
11	HG3	HG3
11	PHASE1	PHASE1
11	PHASE2	PHASE2
11	PHASE3	PHASE3
11	NTC1N	NTC1N
11	NTC1P	NTC1P



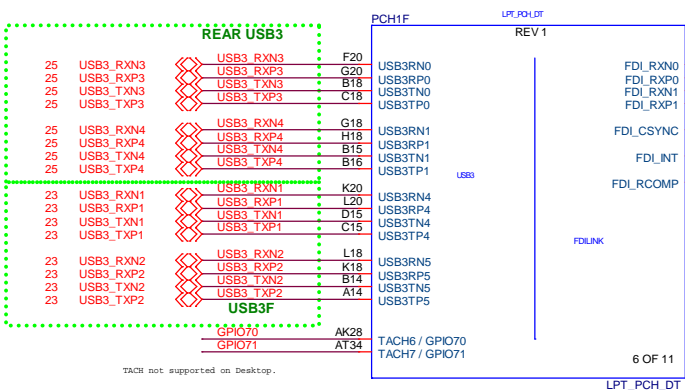
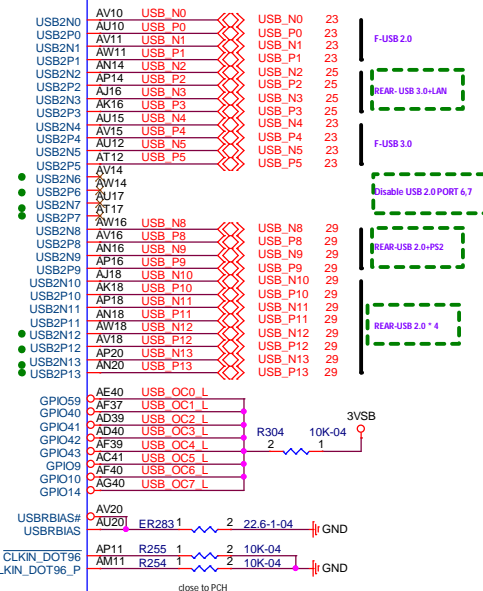
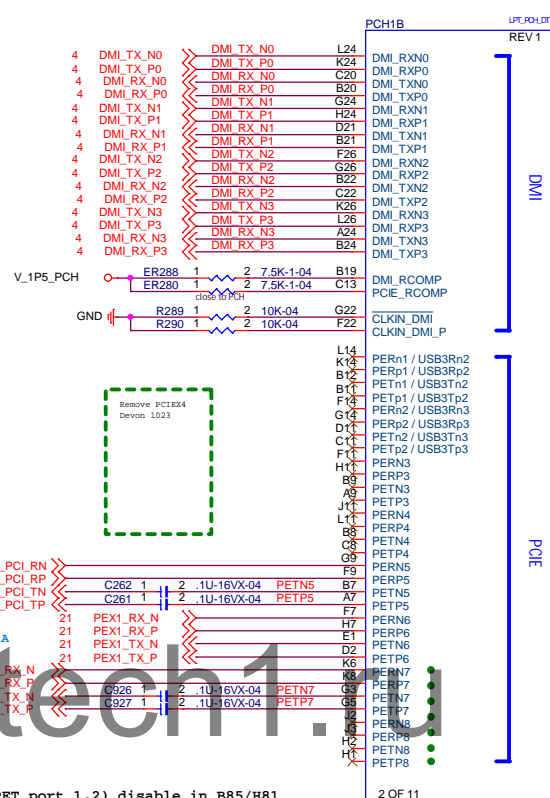
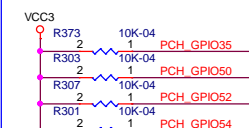
PCH DAC power



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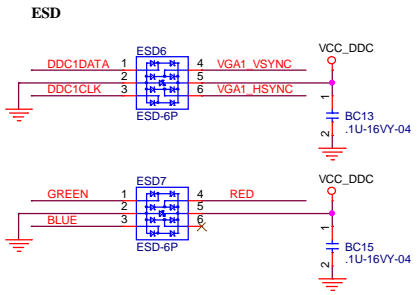
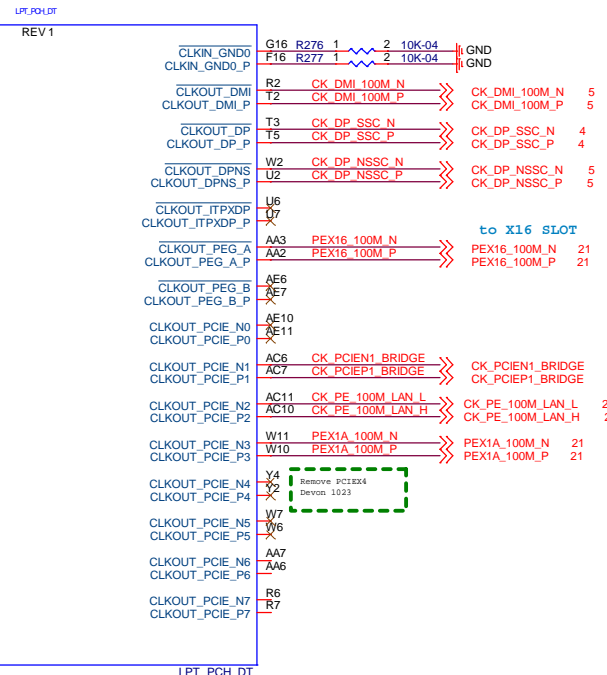
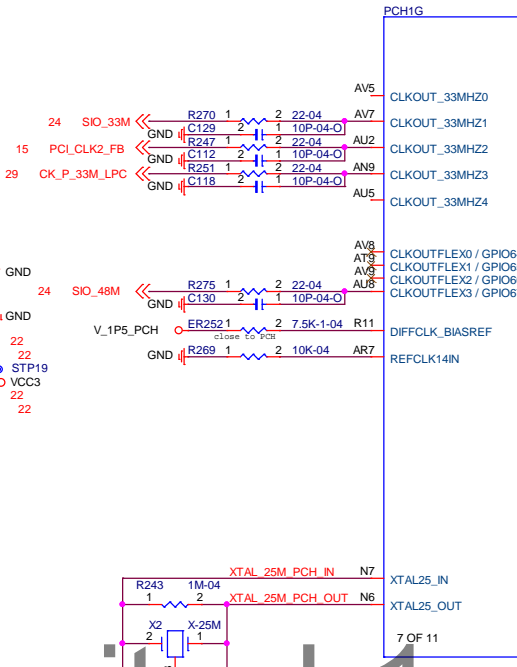
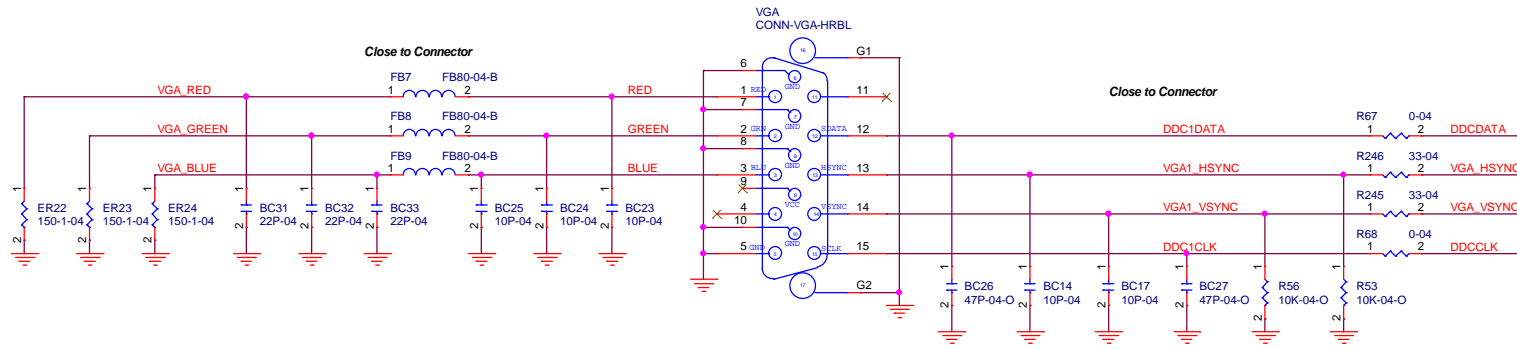
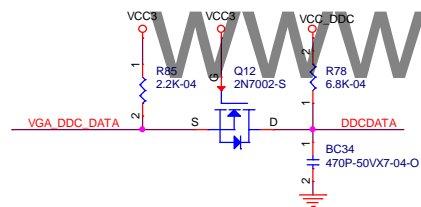
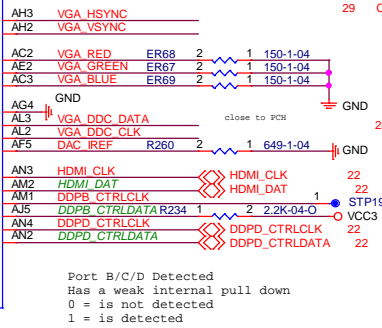
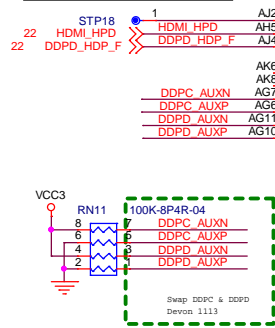


```
GPIO53 : DT shouldn't be pulled-down
GPIO55 : TOP-BLOCK swap override when LOW
```

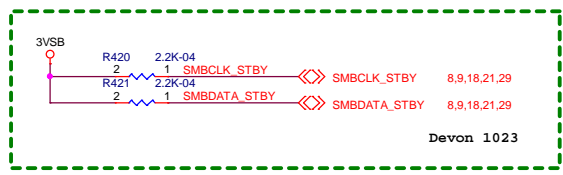
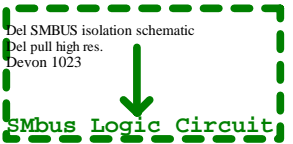
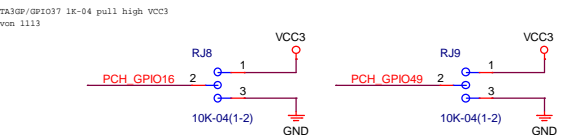
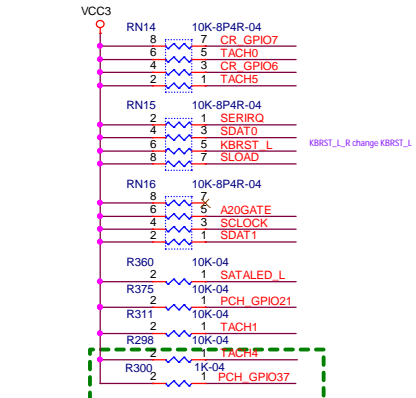


```
USB3.0 (PET port 1,2) disable in B85/H81
PET port 7,8 disable in H81
```

BOOT device	GPIO51	SATA1GP/GPIO19
LPC	0	0
SPI	1	1

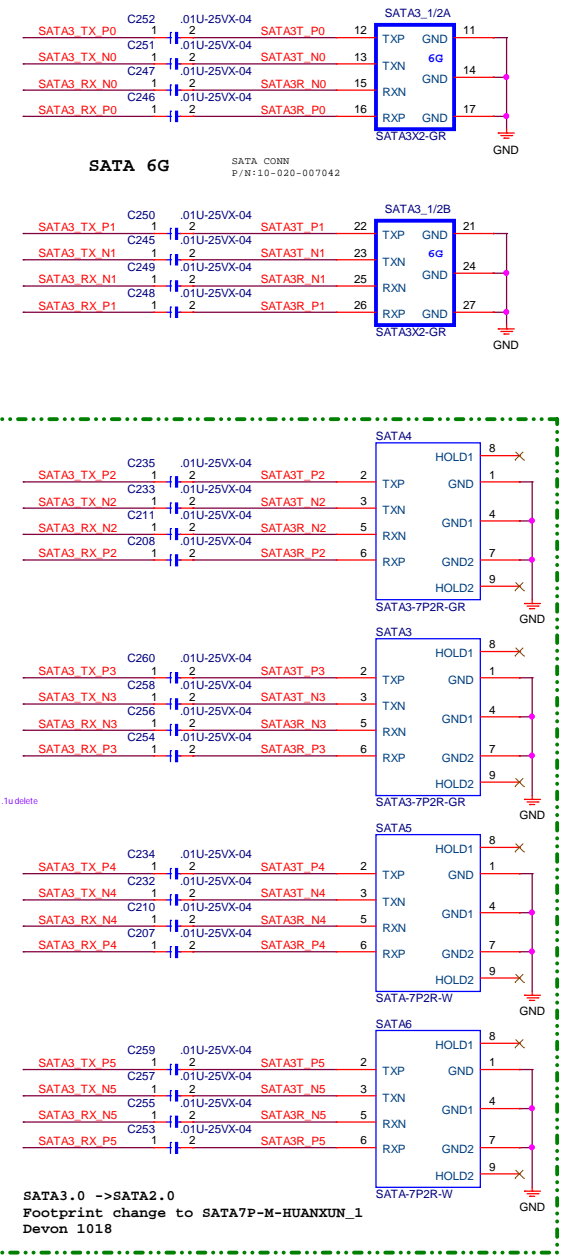
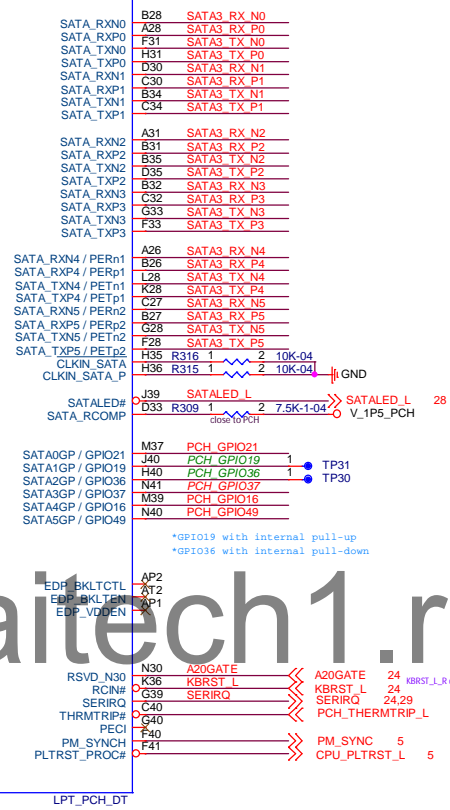


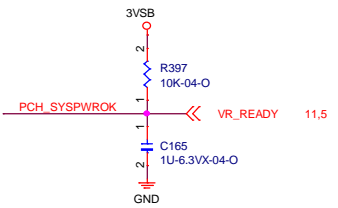
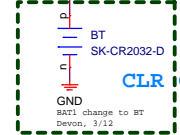
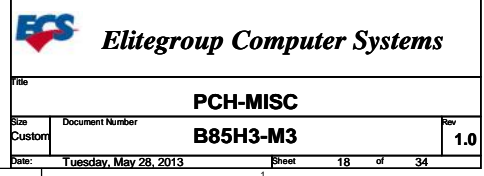
MODE	Ra	Rb
AMT	V	X
NON AMT	X	V

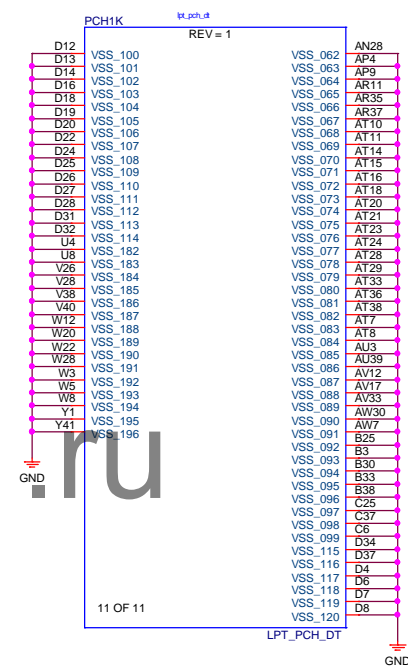
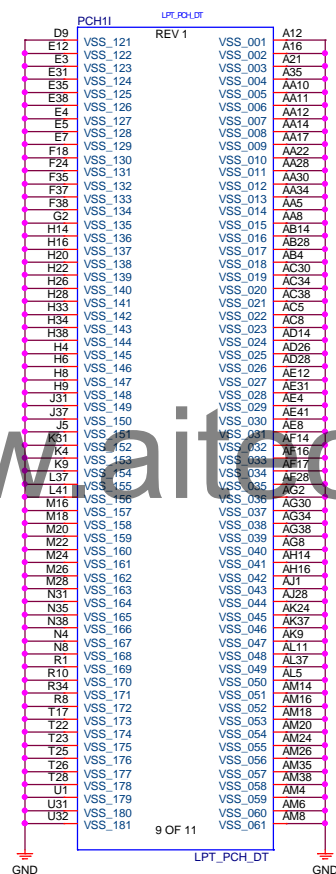
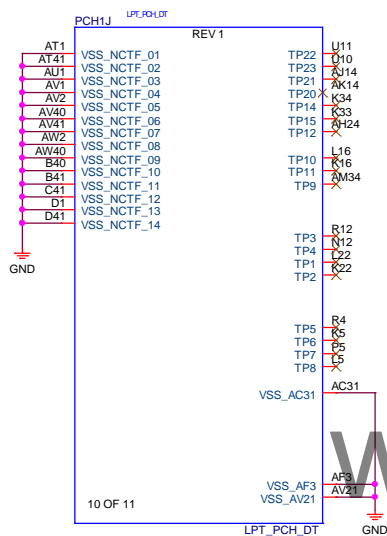


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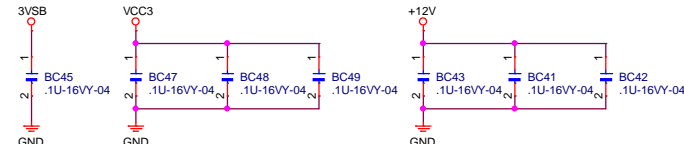
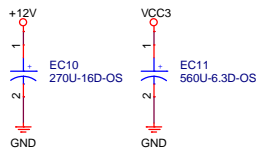
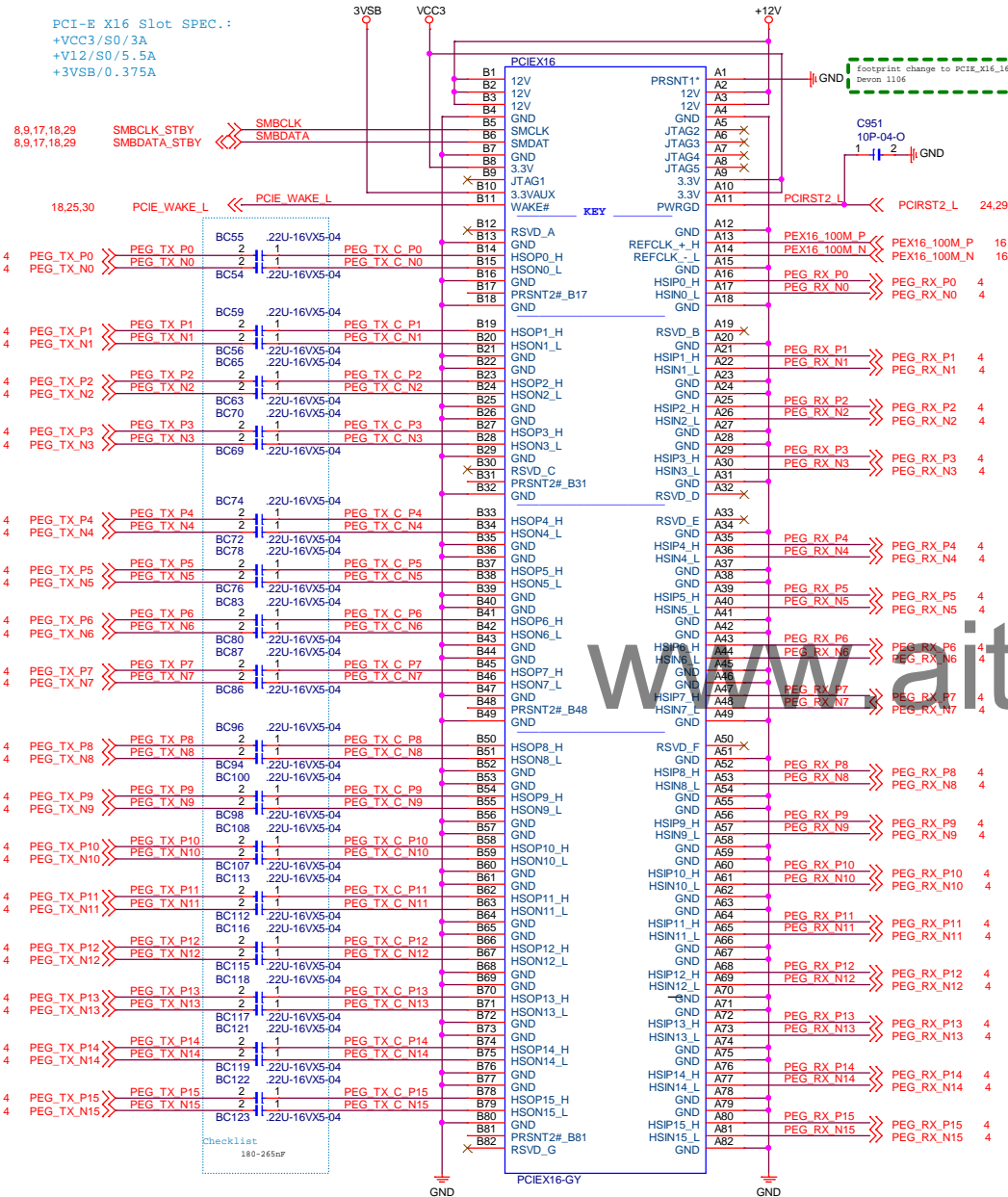
port 2,3 disable in H81
port 4,5 are SATA 3Gb/s in B85/H81



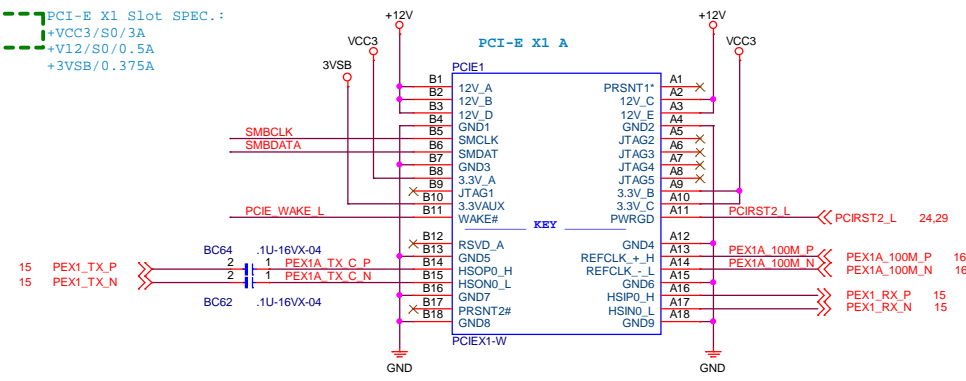




PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A

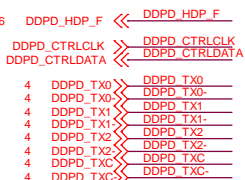


PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

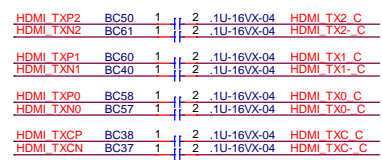
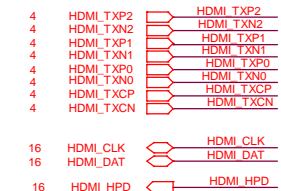
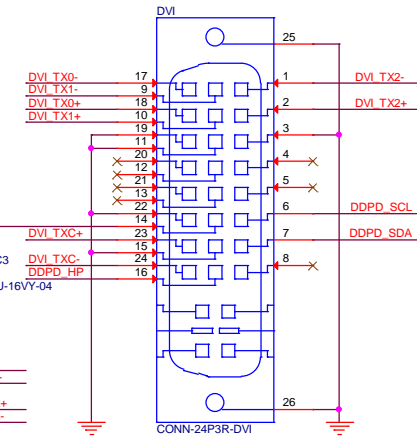
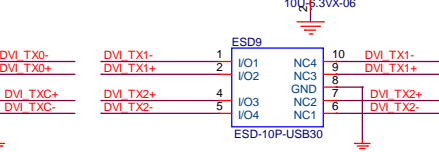
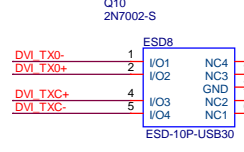
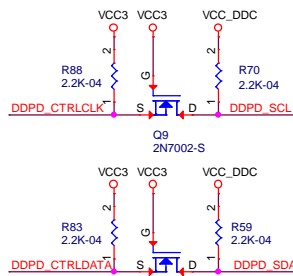
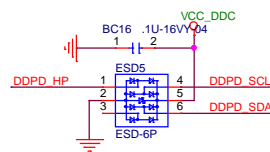
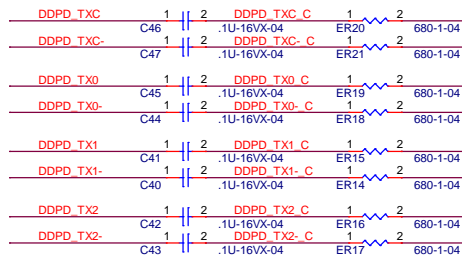
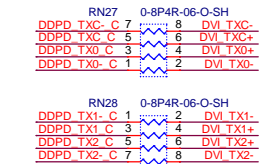


Slot PCI-EX16 / PCI-EX1		
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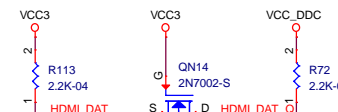
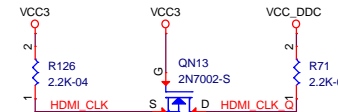
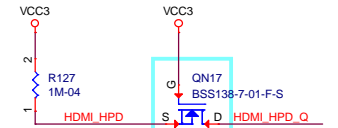
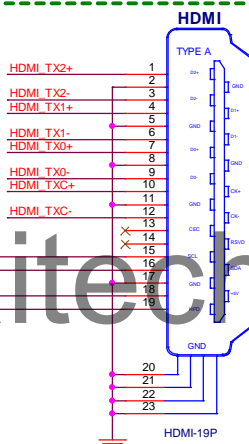
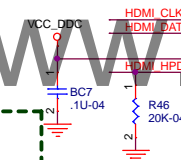
External Connection



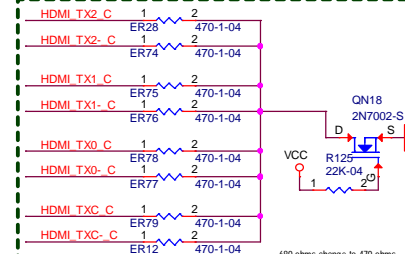
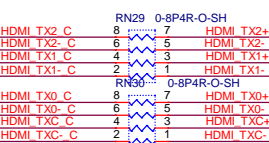
DVI



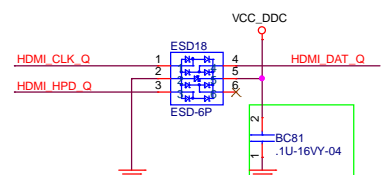
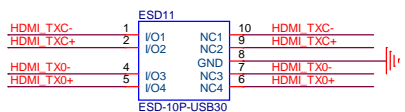
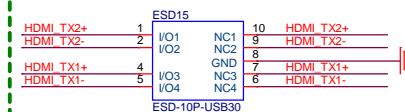
www.aitech1.ru



DEL DP MODULE.
Only save HDMI function.
Devon 1023

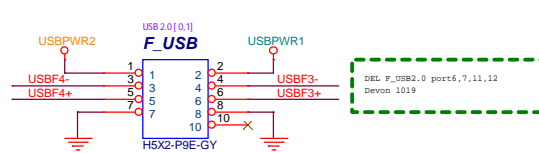
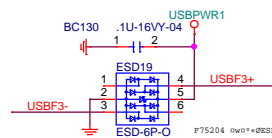
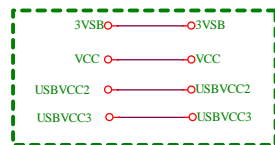


680 ohms change to 470 ohms
to fix HDMI 7-2 issue
Devon 03/01

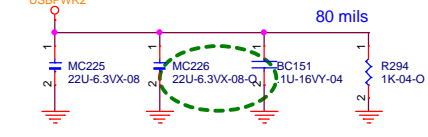
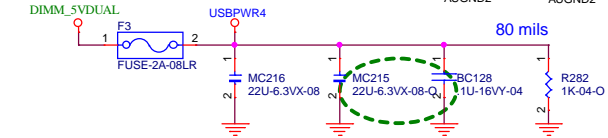
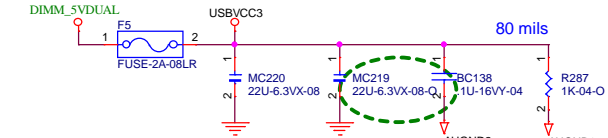
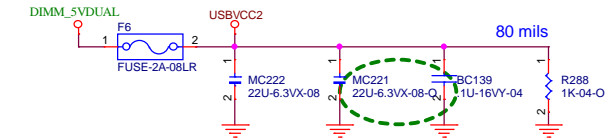
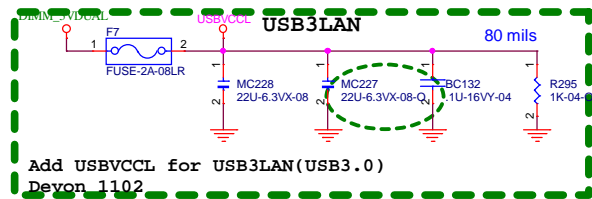


Devon 1102

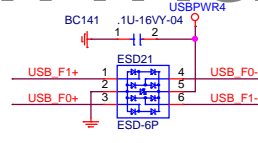
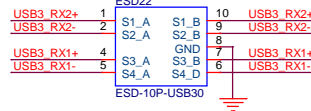
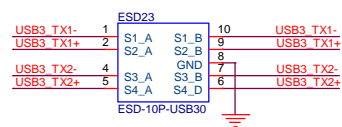
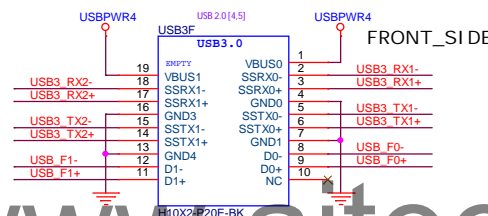
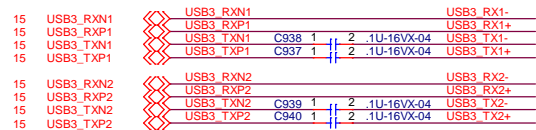
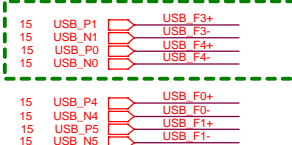
External Connection



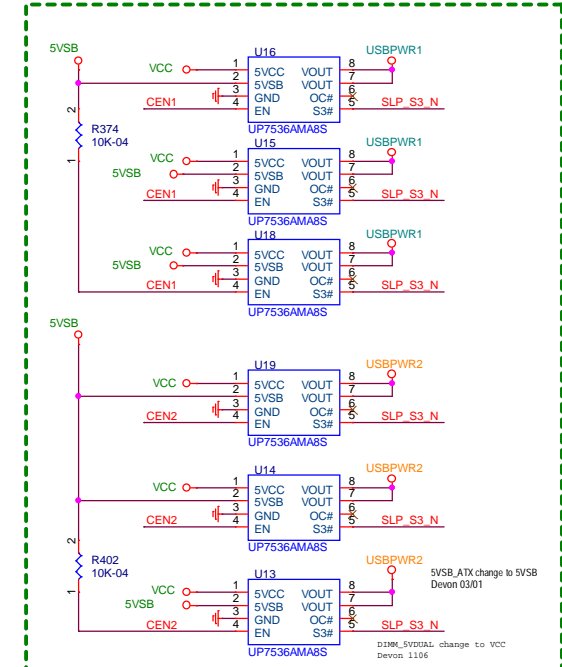
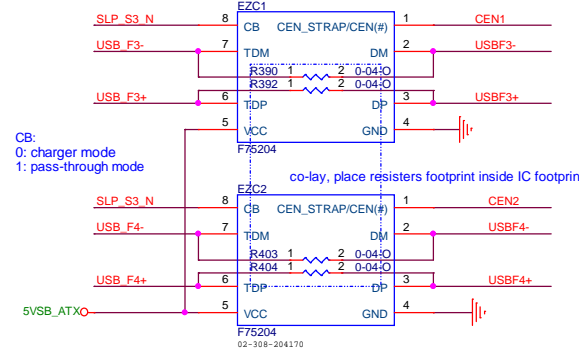
DEL USBPWR3
Devon 1022



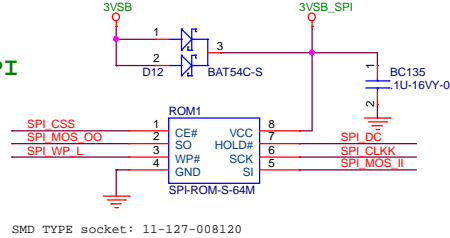
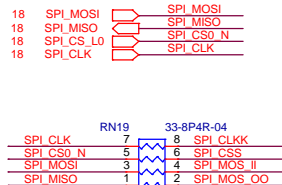
5,13,18,19,24 SLP_S3_L SLP_S3_N



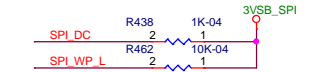
FUSB1 EZ CHARGE



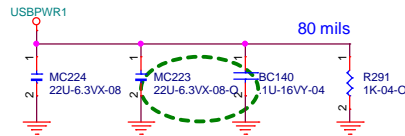
SPI



SMD TYPE socket: 11-127-008120



remove SPI_Debug header
Devon 1106

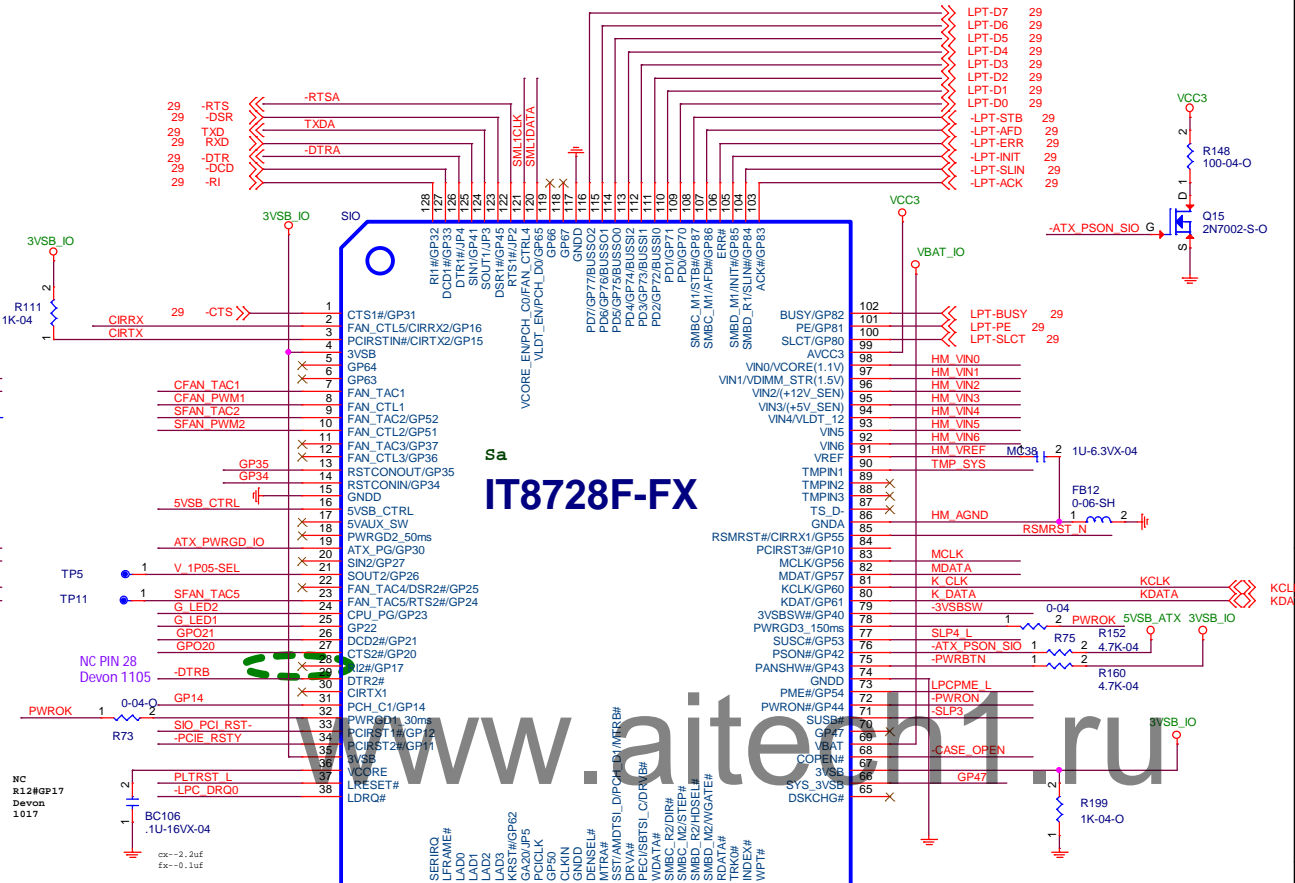
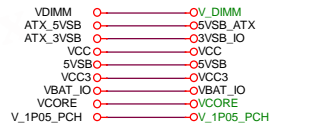


CEN_STRAP:
0: CEN is high active
1: CEN is low active
CEN(#)
asserting for 1 sec. to cut off USBH_PWR
that simulates the re-plugging of USB device
when CB changes

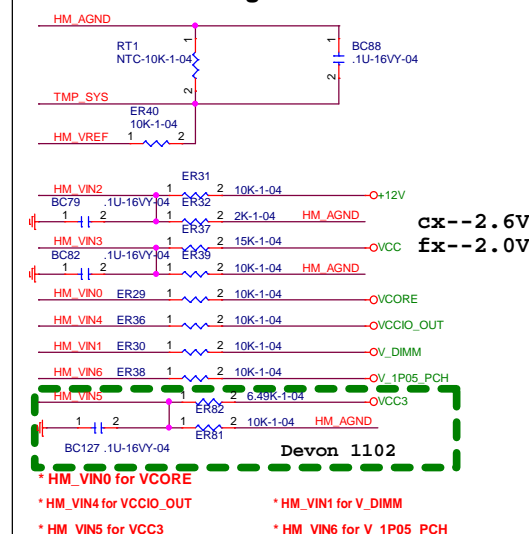
Elitegroup Computer Systems

File		F_USB / SPI	
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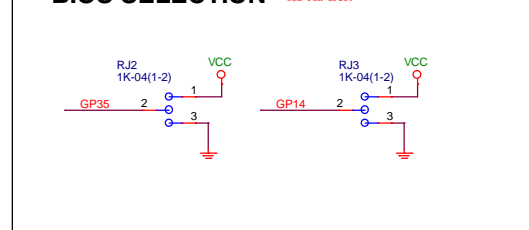
External Connection



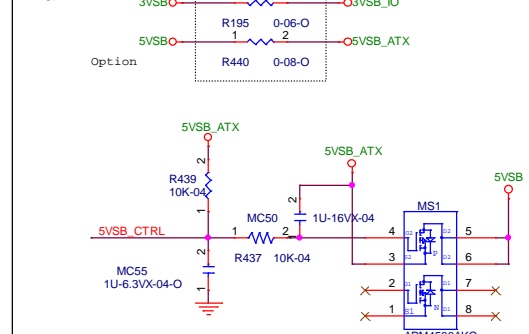
Thermal and Voltage Monitor



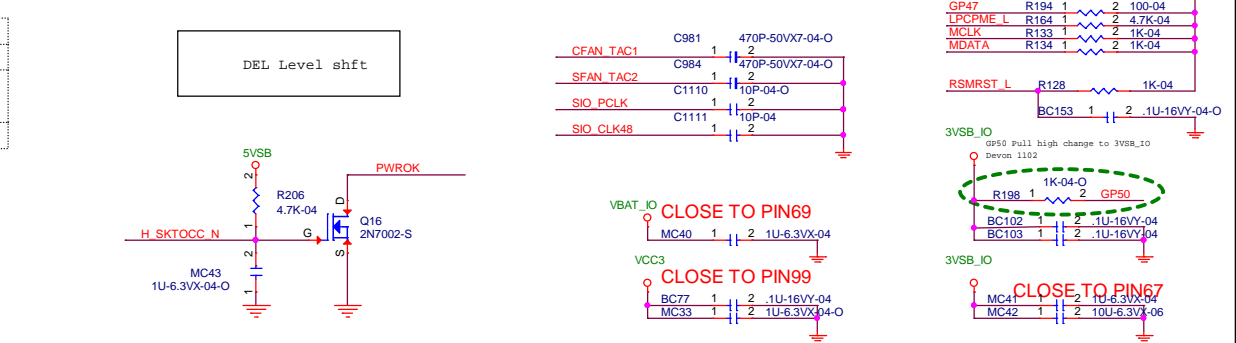
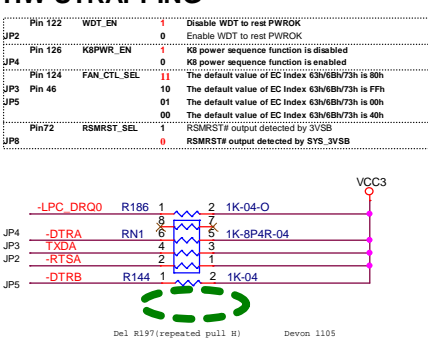
BIOS SELECTION



EuP



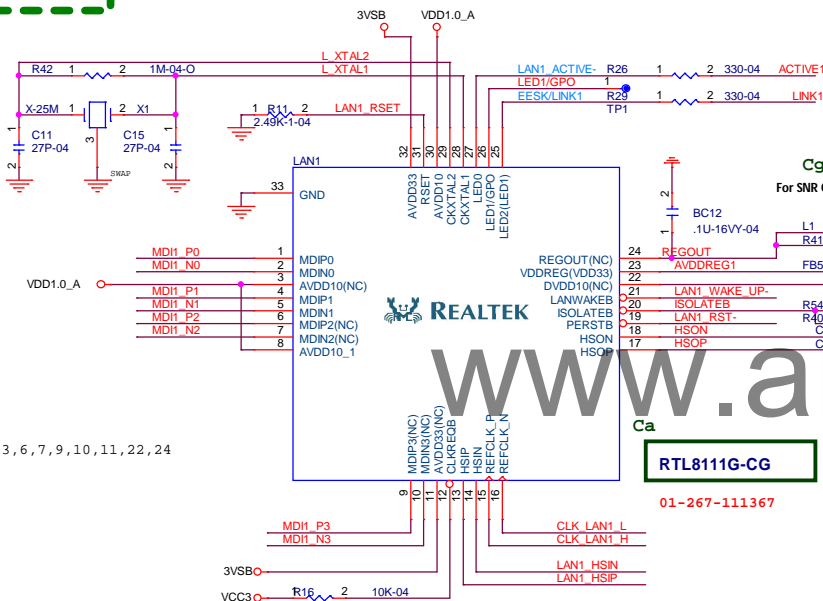
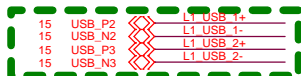
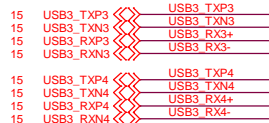
HW STRAPPING



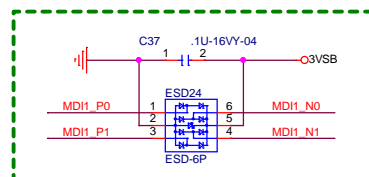
	3VSB		3VSB
	VCC3		VCC3
	USBVCC1		USBVCC1
	AUGND2		AUGND2
18,21,30	PCIE_WAKE_L		LAN1_WAKE_UP
24,30	PCIRST1_L		LAN1_RST-
16	CK_PE_100M_LAN_H		CLK_LAN1_H
16	CK_PE_100M_LAN_L		CLK_LAN1_L
15	LAN_TX_P		LAN1_HS1P
16	LAN_TX_N		LAN1_HSN
15	LAN_RX_P		LAN1_HSP
15	LAN_RX_N		LAN1_HSN



For USB3.0 Add USB3.0
Devon 1019

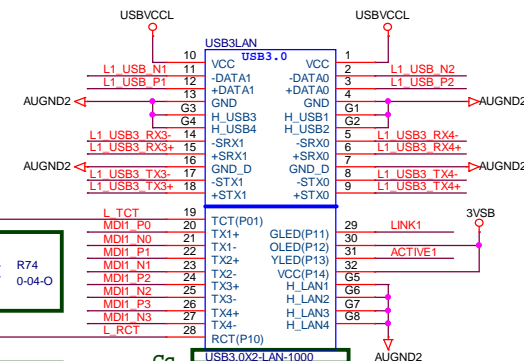
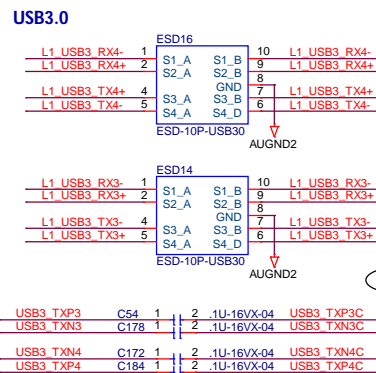
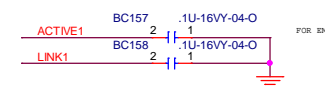
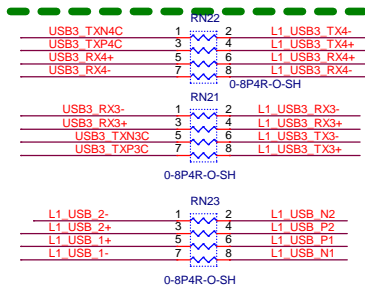
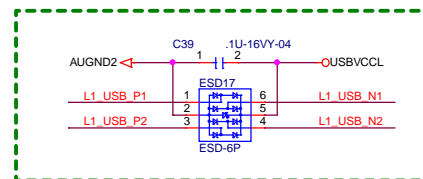
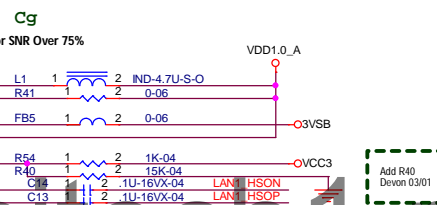
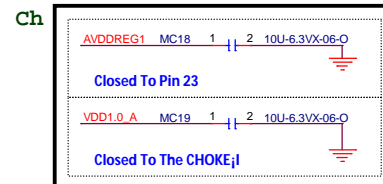
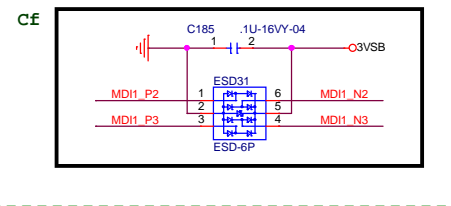


8106E : NC PIN - 3,6,7,9,10,11,22,24



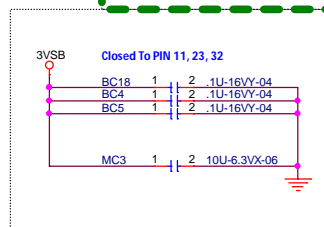
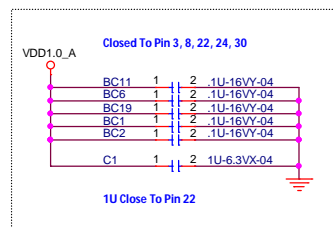
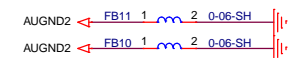
	RTL8111GS-CG (SWR mode) 1000M	RTL8111G-CG (LDO mode) 1000M	RTL8106E-CG (LDO mode) 10/100M
Ca	RTL8111GS	RTL8111G	RTL8106E
Cb	None	None	None
Cc	USB2-LAN-1000	USB2-LAN-1000	USB2-LAN-100
Cd	X	X	V
Ce	0-04	0-04	.01U-25VX-04
Cf	V	V	X
Cg	L	R	X
Ch	V	X	X

DEFAULT

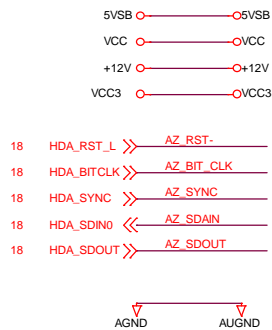


Link: Green on

Active: Yellow blinking



External Connection



* VCC1.5 can remove for non-Intel G4X platform

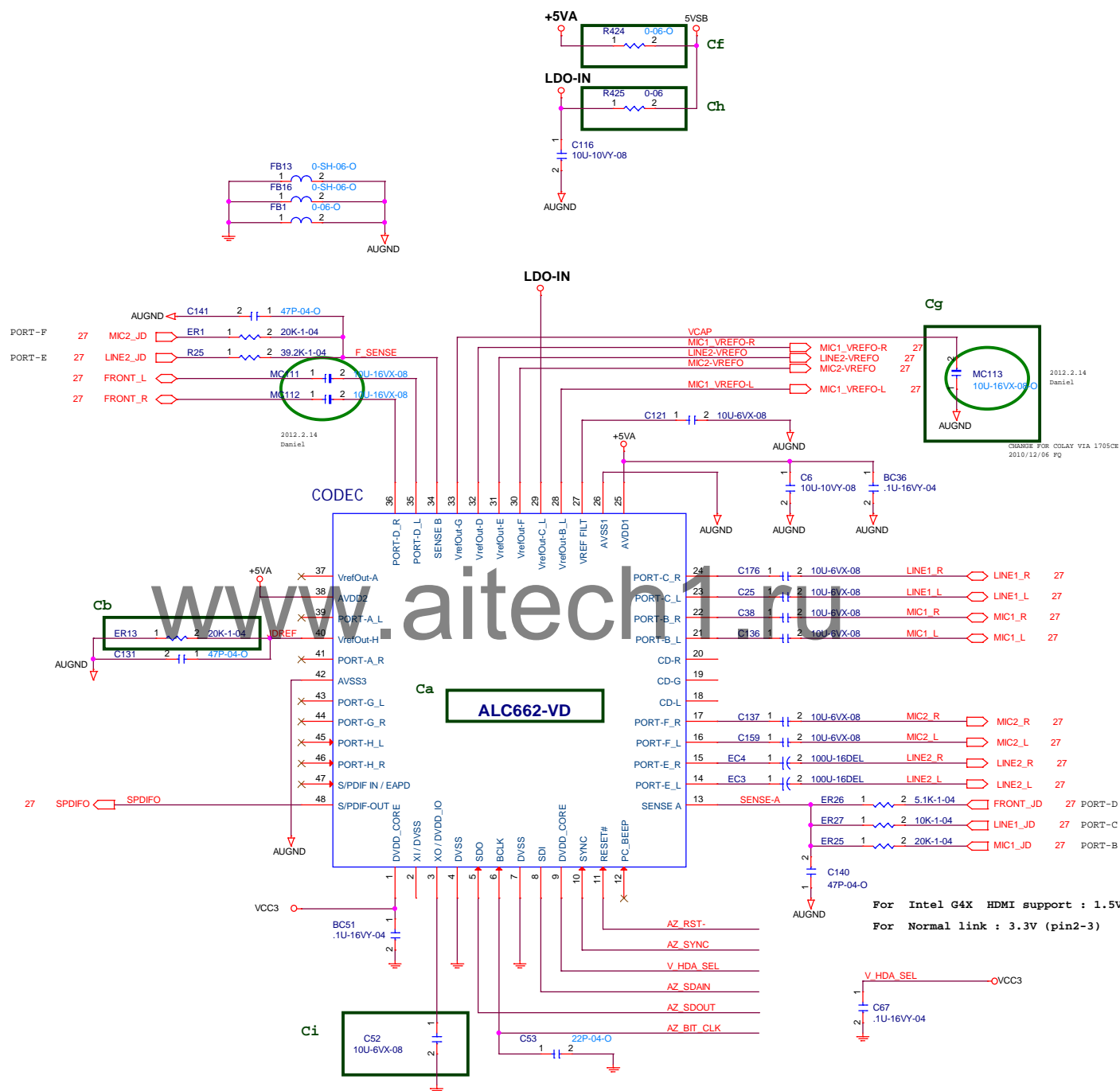
Pin Difference

Pin	ALC662 VD	VT1705CE
3	REG VREF	GPIO1
4	GPIO1	DVSS
25	LDO OUTPUT	LDO VIN
29	LDO VIN	OPTION CAP
33	LINE1 VREF	LDO OUTPUT
37	FRONT VREF ?	NC
38	LDO OUTPUT	LDO VIN
45	DMIC DATA	NC
46	DMIC CLK	NC

BOM Difference

Location	ALC662 VD	VT1705CE
Ca	ALC662-VD0-GR	VT1705CE
Cb	20K-1-04	5.1K-1-04
Cc	V	X
Cd	2.2K-04	3.3K-04
Ce	75-04	16-04
Cf	X	V
Cg	X	V
Ch	V	X
Cl	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.



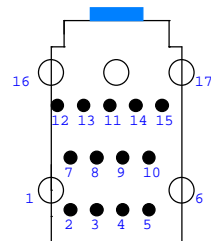
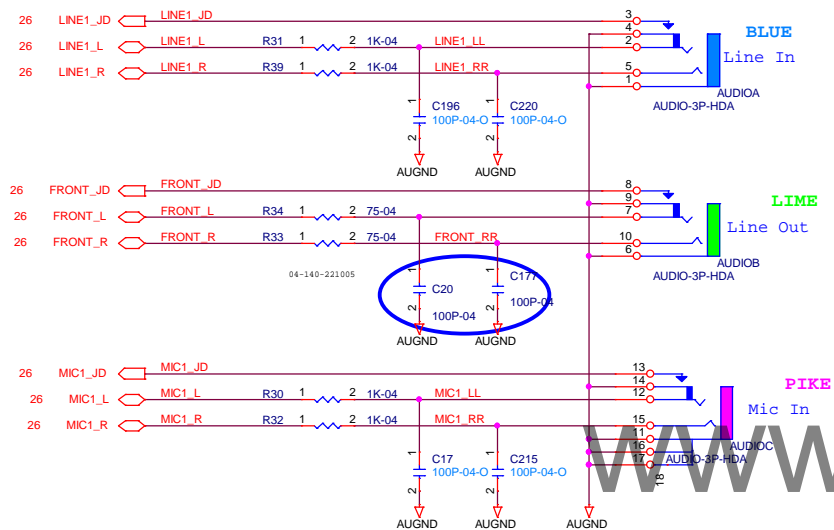
Change ALC892 to ALC662.
Devon 20121016

External Connection

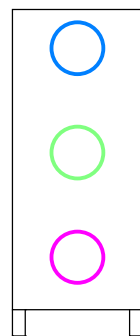
18 FP_AUD_DETECT <-- FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

REAR-AUDIO Non re-tasking for rear panel

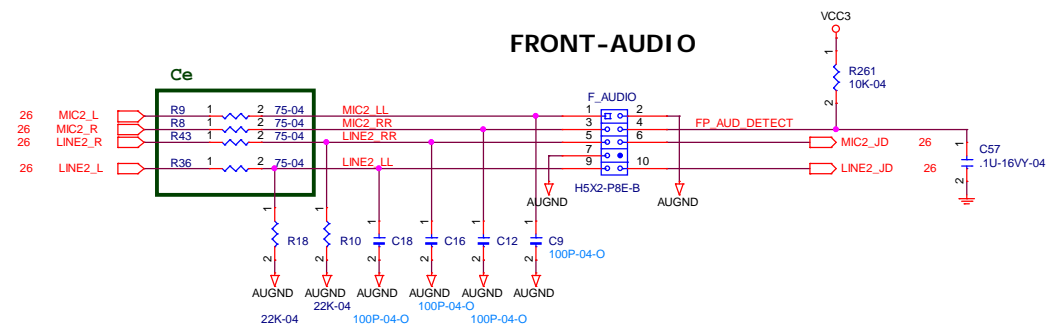


TOP VIEW

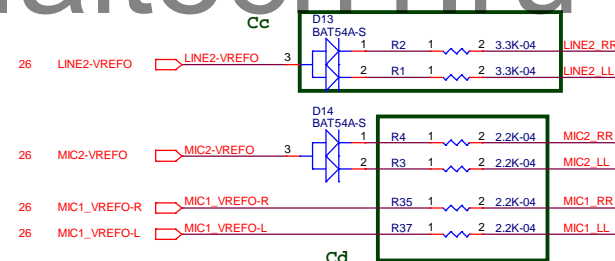


FRONT VIEW

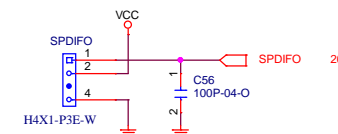
FRONT-AUDIO



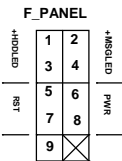
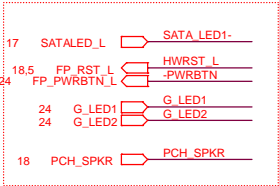
MIC Bias



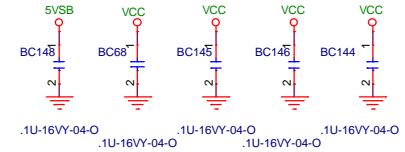
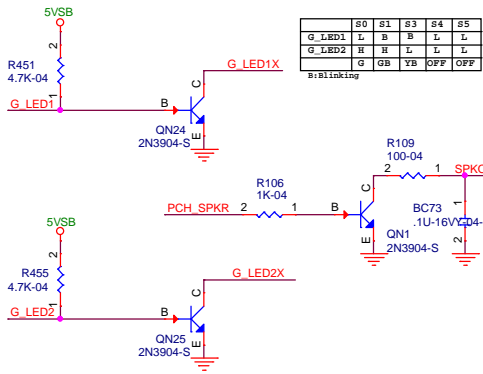
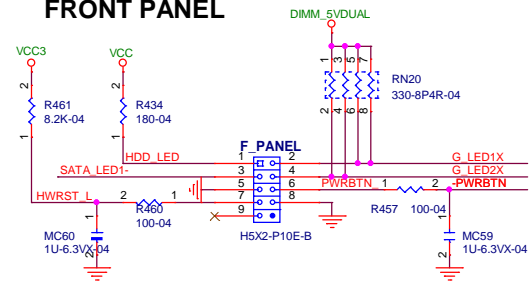
SPDIF-OUT



External Connection

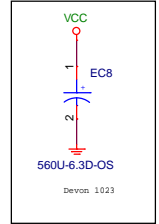
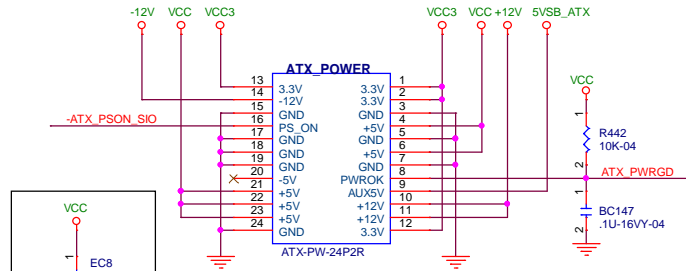
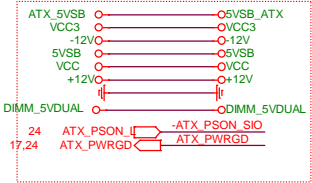


FRONT PANEL



POWER CONNECTOR

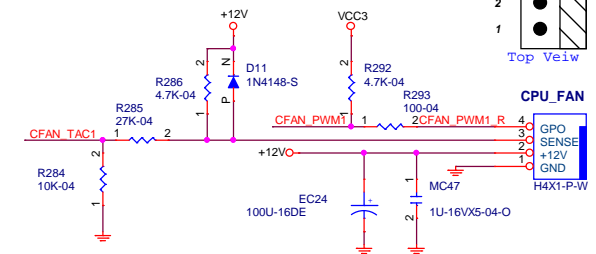
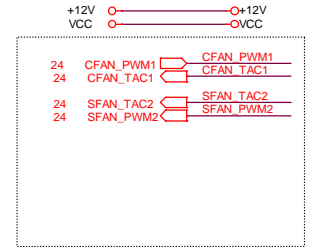
External Connection



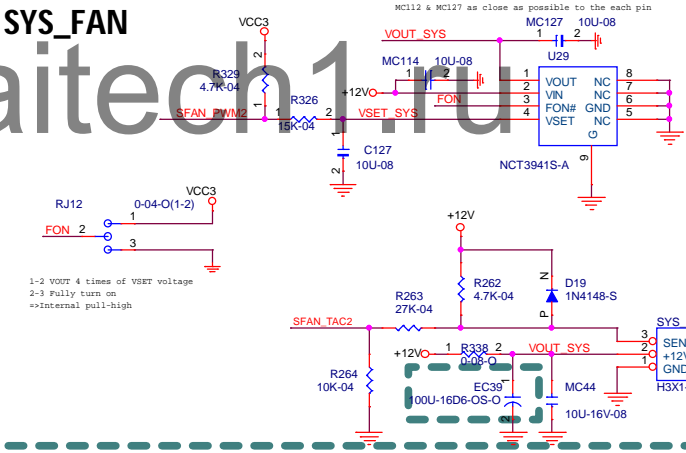
FAN

Kent 1016

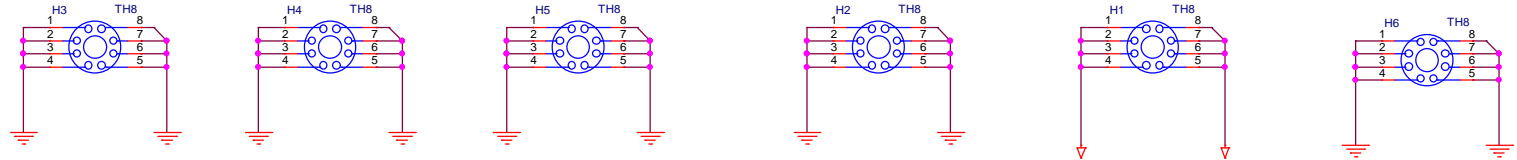
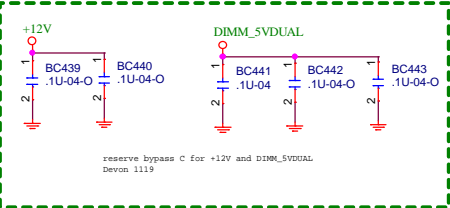
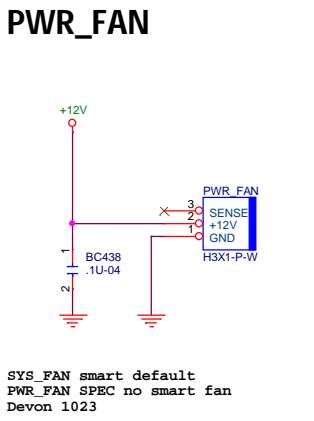
External Connection



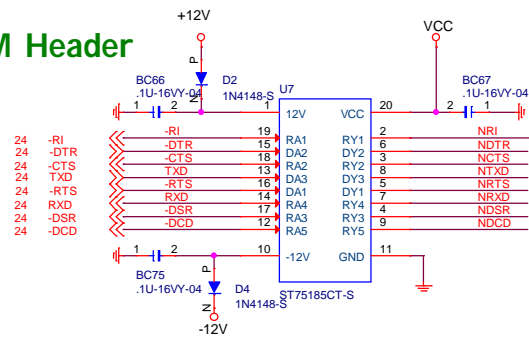
SYS_FAN



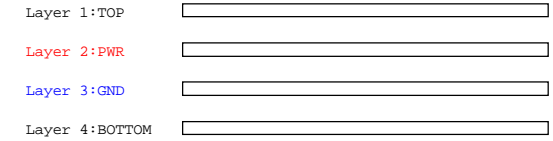
PWR_FAN



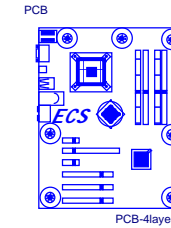
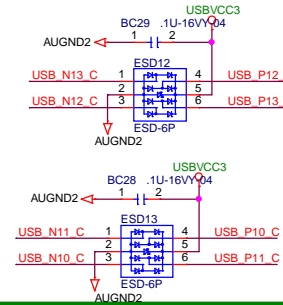
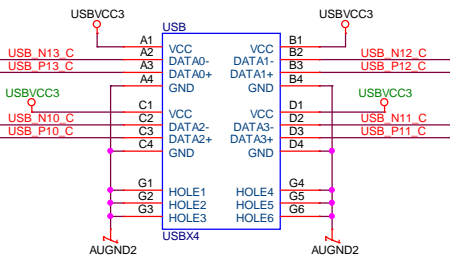
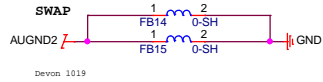
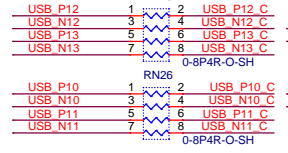
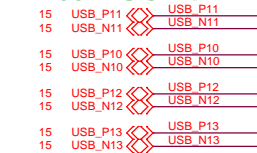
COM Header



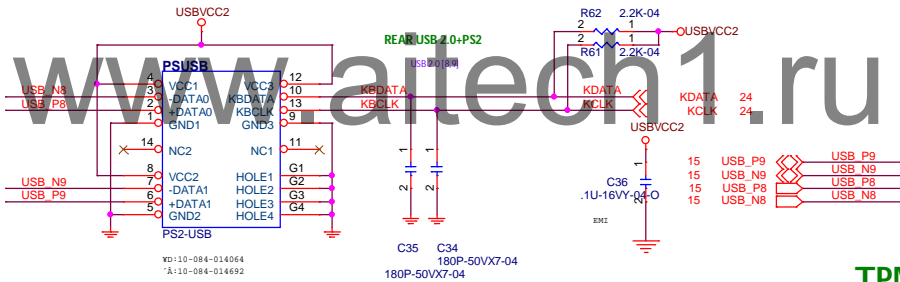
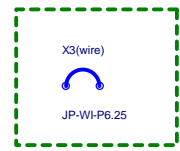
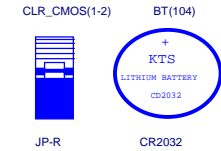
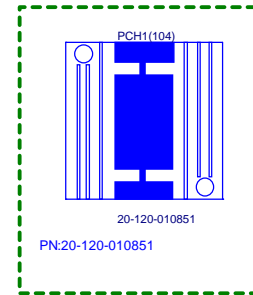
1)Circuit type 1



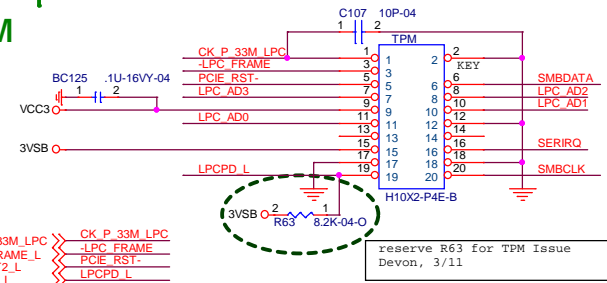
Rear USB4



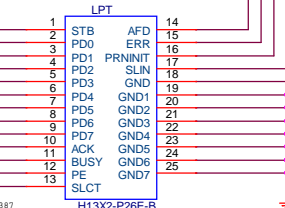
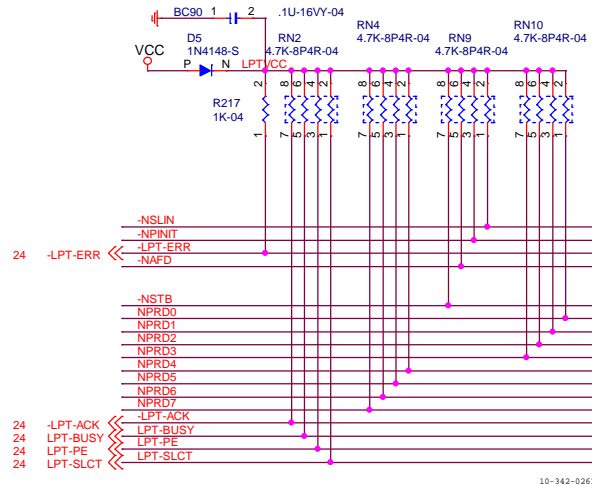
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



TPM



LPT Header



External Connection

VCC
3VSB
VCC3

PAD[31:0]

PAD[31:0]

CK_PCIE1_BRIDGE

CK_PCIE1_BRIDGE

CK_PCIE1_BRIDGE

CK_PCIE1_BRIDGE

CK_PCIE1_BRIDGE

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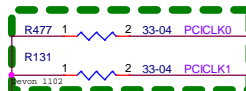
CK_PCIE1_BRIDGE

CK_PCIE1_BRIDGE

CK_PCIE1_BRIDGE

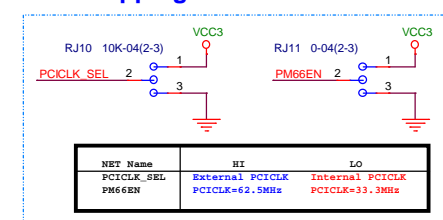
CK_PCIE1_BRIDGE

PCB layout note:
Connect to PCIe
PERST# Signal



ADD PGNT1#, PREQ1#, PCICLK1
Devon 1017

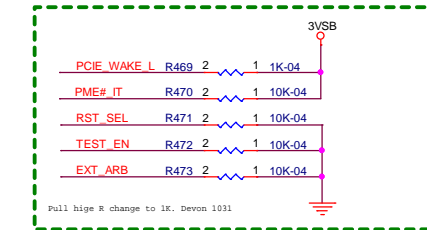
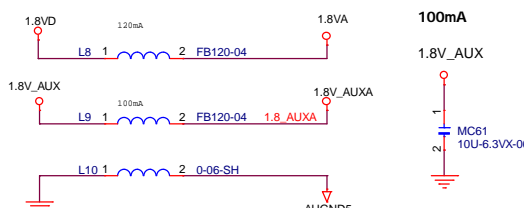
HW Strapping



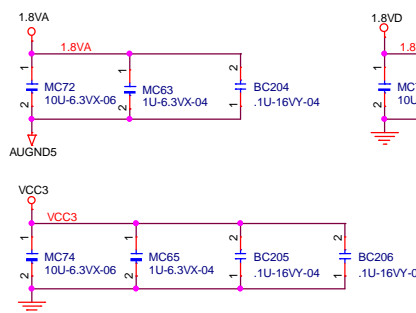
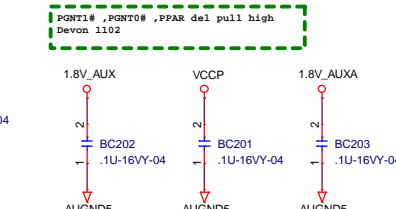
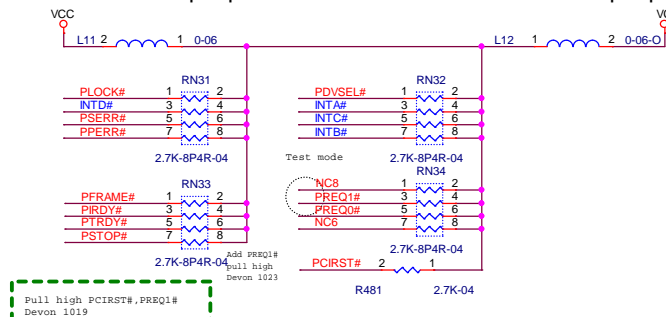
NET Name	HI	LO
PCICLK_SEL	External PCICLK	Internal PCICLK
PM66EN	PCICLK=62.5MHz	PCICLK=33.3MHz

PCIe BUS 3.3_AUX Power

1.8V_AUX Power source



PCI BUS 5V external pull up



PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)

PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)

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External Connection

VCC 0 -VCC
3VSB 0 -3VSB
VCC3 0 -VCC3
-12V 0 -12VD
+12V 0 -+12VD

PCI CHIP

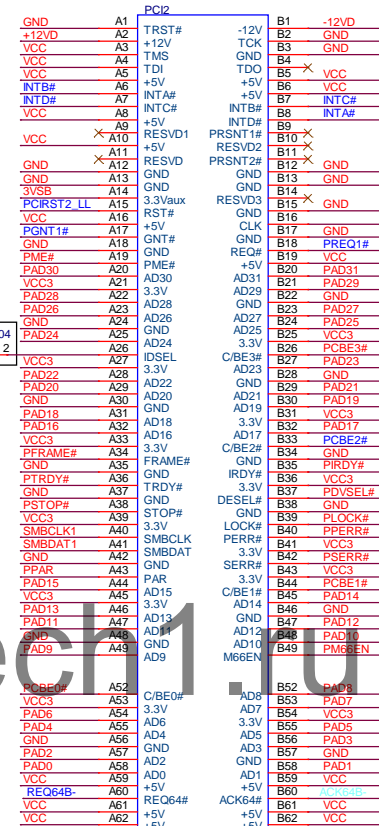
PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

SPI ROM Circuit

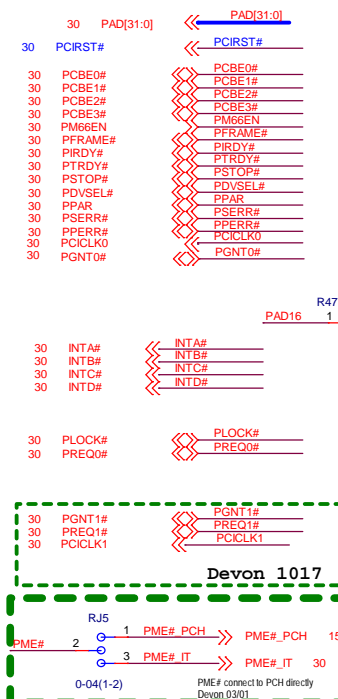
PCI1



PCI2

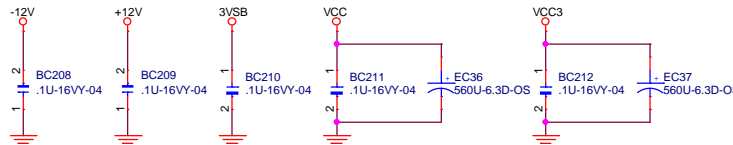
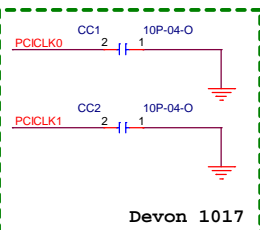
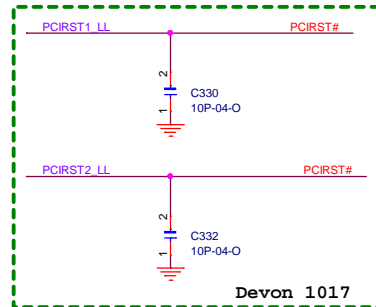
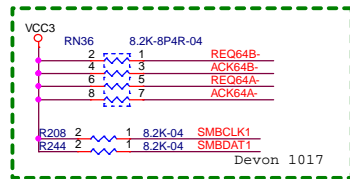


Add PCI2
Devon 1017



PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD

PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA



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ATX P/S WITH 2A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX4P 12V +/-5%

Switching RT889A 3 phases

Vcore TDC:70A

5VDUAL P/N MOS

Switching APW8819QAI-TRG

VDIMM_1.5V

25Amax

DDR3 DIMM 1600MHz (4)	
VDIMM	11A(TDC)
VDIMM_VTT	1A

DDR_VTTR 0.75V

1.1Amax

Switching RT8068A

OP Linear

ME_1.05V 1Amax

PCH_1.5V 0.2Amax

OP Linear

PCH_1.05V 5Amax

Intel Haswell CPU		
VCORE	SVID	105A(95W)
VDIMM	1.5V	4.5A
VCCIO_PCH	1V	TBD

Intel Lynx Point (TDP 4.1W)		
VCC	1.05V	1.29A
V_PROC_IO	1.05V	4mA
VccIO	1.05V	3.629A
VccCLK	1.05V	306mA
VccASW(ME)	1.05V	670mA
VccADAC1_5	1.5V	70mA
VccVRM	1.5V	179mA
VccCLK3_3	3.3V	55mA
VccADAC3_3	3.3V	13.3mA
VccSPI	3.3V	22mA
VccDSW3_3	3.3V	15mA
VccSUS3_3	3.3V	261mA
VccSUSHDA	3.3V	10mA
VccRTC	3.3V	6uA(G3)
DcpSUS1	1.05V	98mA
DcpSUS2	1.05V	28mA
DcpSUS3	1.05V	476mA

Battery 3V

LANRT8111G		
AVDD33	3.3V	TBD
VDD1.0_A	1V	TBD

FAN		
CPU_FAN	+12V	TBD
SYS_FAN	+12V	TBD

SIO IT8728		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
Battery 3.3V	3.3V	TBD

AUDIO ALC662		
DVDD 3.3V	3.3V	11mA
AVDD	5V	42mA
Internal LDO		

DIMM_5VDUAL
DIMM_5VDUAL

USB_DUAL

USB_DUAL

MINE PCIE / mSATA Slot per	
3.3Vaux	1.1A(S0)
1.5V	375mA(S0)

each USB3.0	
VDD	5VDual
	0.9A

each USB2.0	
VDD	5VDual
	0.5A

PS/2	
5VDual	275mA

PCI Slot per	
3.3V	7.6A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

ATX_3VSB

VCC3

VCC3

ATX_5VSB

